analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

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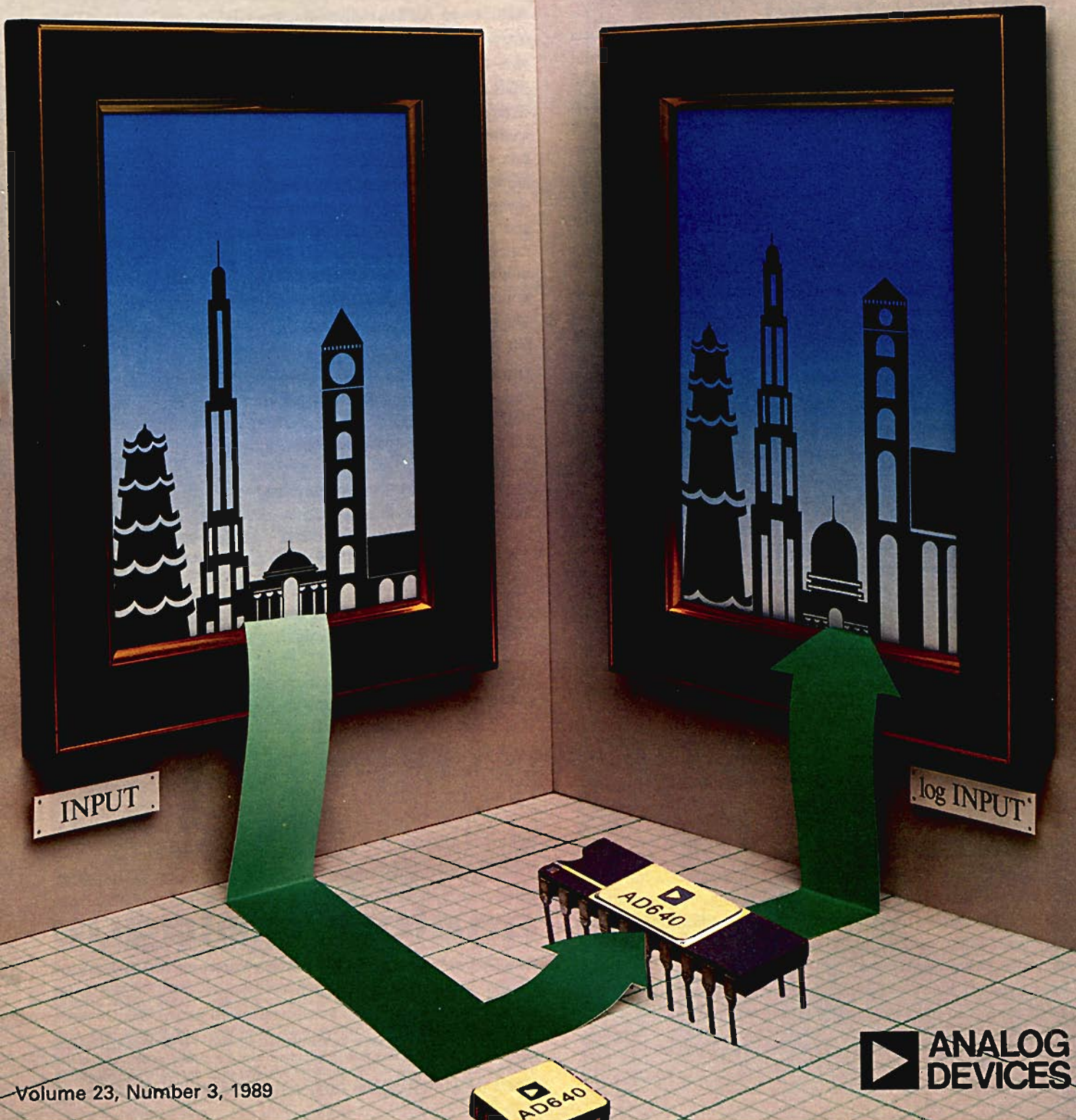

Volume 23, Number 3, 1989

ANALOG DEVICES

Editor's Notes

PRODUCT PROLIFERATION HARNESSED

Throughout a lifetime of observation, the commandment from *Genesis*, "Be fruitful and multiply," has appeared to this observer to harbor a mixed blessing. On the one hand, unchecked, it poses a threat to the environment; on the other, it is the key to rejuvenation. White cells doing it usually stop disease; cancer cells propagate disease.

In this brief essay, we'll discuss how proliferation of products gives us the joys of choice and range, the woes of cataloguing and selection. We wind up on a hopeful note by pointing to Bill Schweber's article on page 20 about the Component Selection Disk, wherein the computer, searching quickly to find the paydirt areas of best specs and least cost, offers hope of reducing the pain while realizing the latent benefits of product proliferation—when you design with components from Analog Devices.

In 1952, we were present at the birth of the first commercial differential op amp, the Philbrick K2-W. It had vacuum tubes, a ±50-volt output swing, at ±1 mA, 1 mV/°C drift, and other specs not really relevant to this discussion. As engineers and scientists learned what op amps could do, they wanted them; but they also wanted ±100-V output (a need satisfied by the K2-X), chopper stabilization (satisfied by the K2-P), more output current (satisfied by the K2-B booster follower); then they wanted it all in one device (the USA-3 Universal Stabilized Amplifier).

Those were the generations of modular vacuum-tube op amps ("there were giants in those days"). But as with the dinosaurs, natural selection took its inevitable course, and proliferation of vacuum-tube amplifier types never reached the problem stage. Small, low-powered, low-cost op-amp modules containing transistors appeared on the scene; they spread rapidly, but were prevented from runaway proliferation by the appearance soon of IC op amps. Now, after a whole quarter-century of IC op-amp development we see the benefits—and costs—of proliferation:

We see: ordinary op amps (741's), low-bias-current FETs, low-drift types, wide-bandwidth op amps, fast-settling op amps, fast-slewing devices, combinations of the above, multiple op amps on a chip, differing performance grades of generic types, differing temperature ranges, packages, supply voltages, micropower op amps, transimpedance op amps, op amps employing new processes like complementary bipolar, etc. All good stuff, but Egad! To the neophyte designer (and certainly to this hoary head as well), the number and variety of types to choose among must be reminiscent of the Tower of Babel.

Many designers deal with the problem by using just a few types for everything, ignoring the possibility of savings of cost or space; or they put themselves in the hands of an Applications or Sales Engineer, who must base his advice on incomplete knowledge of the specific problem; or they (or their Component Engineers) spend endless hours searching, tabulating, comparing—and still not knowing how close they may be to the "best choice."

For all of these, there is now hope: not a Saviour, but a saver—of time, money, and the agonies of choice.

Dan Sheingold

THE AUTHORS

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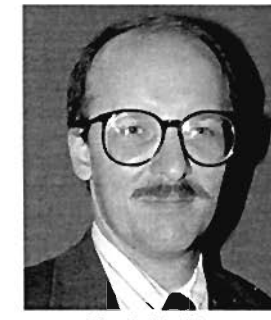
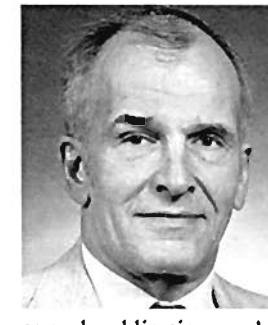


Bob Clarke (page 3), a Product Marketing Engineer in the Linear Group at ADS for amplifiers and analog signal-processing products, has a BSEE from MIT. Before joining Analog, he worked at *Electronics Test* and *EDN* Magazines and M/A-COM. He has written numerous articles for a variety of publications. His hobbies include sailing, windsurfing, reading, and amateur radio (N1RC).



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(More authors on page 22)

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MONOLITHIC DC-TO-120-MHz LOG-AMP IS STABLE AND ACCURATE

AD640 Provides Total Calibration over Wide Temperature Ranges Can Be Paired for up to 95-dB Dynamic Range

by Barrie Gilbert and Bob Clarke

The AD640* is a monolithic laser-trimmed multi-stage logarithmic amplifier ("log amp")—a *complete, calibrated measurement system* comprising five 10-dB stages with paralleled current outputs that produce a device output current precisely proportional to the logarithm of the input voltage. Deviating only ±0.6 dB from the ideal function, the AD640 is designed from the outset to exhibit high stability with temperature through the use of accurate nonlinear-circuit design principles. Fabricated on a high-speed bipolar-plus-thin-film process, it draws only 220 mW from ±5-volt supplies and is available for industrial and military temperature ranges in a choice of 20-pin DIP and LCC packages. Prices start at $63.59 (100s).

Log amps have maximum incremental gain for small signals; the gain decreases in inverse proportion to the magnitude of the input. This relationship permits the amplifier to accept signals with a wide input dynamic range—as much as 56,000:1 for two cascaded AD640s (Figure 1)—and compress them substantially. Typical applications include amplification and demodulation in radar and fiberoptic receivers—and providing signal-strength measurements for spectrum analyzers, r-f voltmeters, chromatographs, and other instruments.

The AD640 is based on the idea of *progressive compression* of a signal as it passes through several amplifier/limiter stages. Each cascaded stage provides voltage amplification and a separate full-wave-rectified current output proportional to the input. The AD640 (Figure 2) comprises five cascaded amplifier/limiter stages, each having a small-signal gain of 10 dB (i.e., ×3.162) and a 3-dB bandwidth of 350 MHz. The summed currents represent the logarithm of the cascaded (multiplied) gains.

Unlike log amps that have been available recently—most of which are either single-stage ICs† and hybrids, or hard-to-trim assemblies of single stages—the AD640 raises the level of integration and provides high accuracy with guaranteed specifications, eliminating user calibrations or trims. The input and output of each stage are differential throughout, an important advantage in view of the extremely high gain-bandwidth product and single-chip construction.

As noted, each stage has a full-wave rectifier in the form of a differential-input-and-output transconductance (V-to-I), which converts the input at each amplifier to current proportional to the local magnitude of the signal, but independent of the sign. The sum of the current outputs of all the limiters closely approximates the logarithmic function. In most rf applications, this current is converted back into a voltage and low-pass filtered to recover the envelope (or *video*) content of the signal. Differing from the commonly used half-wave rectifier, a full-wave rectifier results in a ripple at *twice* the input frequency; this considerably simplifies the design of low-pass filters when high video bandwidths must be achieved. Also, with the differential outputs brought to dedicated pins, no rf currents flow in the supply lines; this simplifies decoupling and lowers the risk of instability.

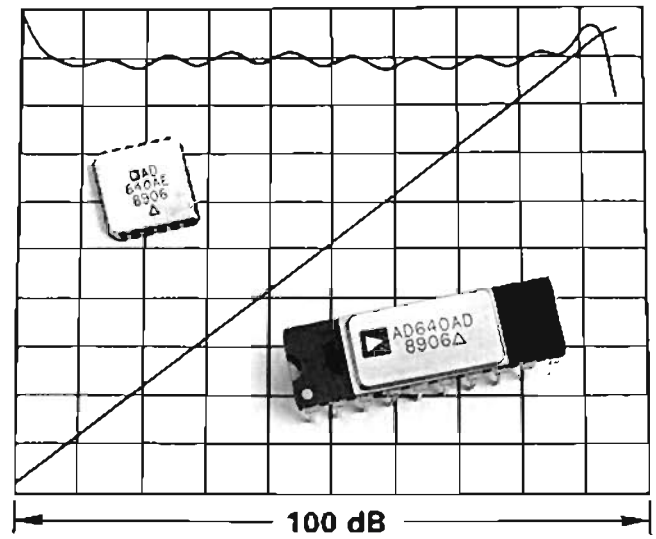

Figure 1. A complete, calibrated measurement system, the AD640 provides 5 10-dB gain stages. It operates from −55 to +125°C, is available in 20-pin DIP or LCC packages.

Although the AD640 responds only to the amplitude of V_{IN}, and not its sign, it can be used in non-demodulating applications where the signal is unipolar, such as the output from a microwave Schottky-diode detector.

In a 1-to-80 MHz bandwidth, a single AD640 provides 46 dB of conversion range, while two devices provide a noise-limited range of 80 dB; the range increases to 95 dB (from −97 dBm to

*Use the reply card for technical data.
†See the description of the AD9521* in *Analog Dialogue*, 22-1, p. 18.

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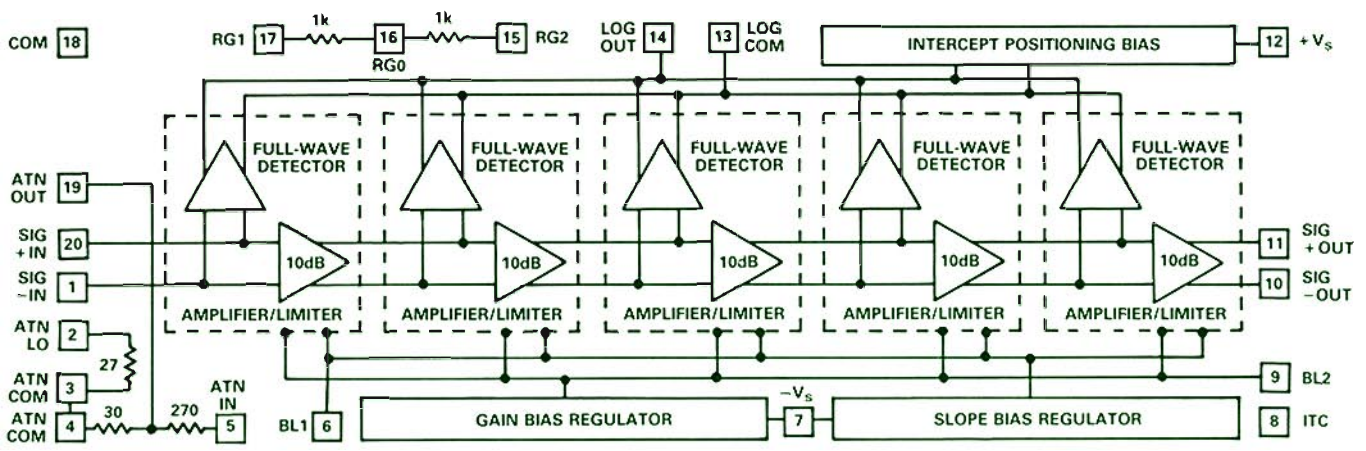


Figure 2. Block diagram of the AD640. The pin configuration and chip layout follow the general form shown here.

−2 dBm) in a 20-Hz-to-100-kHz bandwidth (Figure 3). Note that −97 dBm (50 Ω) corresponds to a signal of only 3 μV rms. In 50-MHz-to-150-MHz operation (that is, 100-MHz bandwidth), it is still possible to provide a 70-dB range with good accuracy. The AD640's on-chip attenuator can shift the dynamic range upward by 20 dB, allowing inputs of up to +18 dBm to be handled directly at the IC pins—a useful feature.

The AD640's topology is frequently used in video (or "baseband") applications, where the instantaneous value of an input of large dynamic range must be compressed to something more manageable, prior to subsequent processing such as A/D conversion. Provided that a log function's inherently (and predictably) high distortion can be tolerated (or mathematically dealt with in later processing), log-amps of this kind can extend the dynamic range of, say, a high-speed 8-bit flash converter to the equivalent of up to 16 bits without seriously impacting bandwidth. For example, a 96-dB dynamic range would be divided into 256 equal increments of 0.375 dB each.

The AD640 is similar in general form to most rf log-amps, but its *accuracy* and *stability* are considerably better than hitherto available. This is always a useful asset—and particularly valuable in multi-channel applications, where tight matching of all channels is essential. Also, the AD640 provides a much more complete solution, including close-tolerance application resistors for voltage scaling of 0.5, 1 or 2 volts/decade (i.e., 25, 50, or 100 mV/dB).

The transfer function of the AD640 is completely specified for a wide variety of input waveforms, not just the sinewave conditions often used for test in rf applications. Thus, calibration is specified for triangle-wave inputs, square waves, pulses, and Gaussian noise. Although well-suited to rf applications because of its on-chip demodulation, the AD640 is dc-coupled throughout; this allows it to be used in LF and VLF systems, including audio measurements, sonar and other instrumentation applications requiring operation to low frequencies *or even dc*.

THE THEORY BEHIND THE AD640

Linear amplifiers and logarithmic amplifiers differ in fundamental ways. A linear amplifier provides gain which is independent of signal magnitude—the large-signal ratio, V_{out}/V_{in}, is the same as the incremental ratio, $\partial V_{out}/\partial V_{in}$. Both can unambiguously be called "gain" in a linear system. On the other hand, a logarithmic amplifier exhibits an incremental (small-signal) gain which is *inversely proportional* to the input voltage magnitude, approaching infinity for very small inputs in the ideal case. While it is acceptable to refer to them as amplifiers, it is also useful to view "log-amps" as a special type of *nonlinear function circuit*, having the input/output relationship

$$V_{out} = V_y \log \frac{V_{in}}{V_x} \qquad (1)$$

where V_{in} is the instantaneous input voltage, V_{out} is the instantaneous output voltage, V_y is a scaling voltage, or *slope voltage*, and V_x is a second scaling voltage, which will be called the *intercept voltage* (because when $V_{in} = V_x$ the output crosses the line, $V_{out} = 0$). Since base-10 logarithms are convenient in the context of decibel quantities, V_y can be also viewed as the *volts-per-decade* factor. Eq. (1) can be differentiated to find the *incremental* (small-signal) gain:

$$\frac{\partial V_{out}}{\partial V_{in}} = K \frac{V_y}{V_{in}} \qquad (2)$$

where K is a constant, here equal to 2.303 (that is, $\log_e 10$). Discussions of "gain" will mean the incremental or small-signal

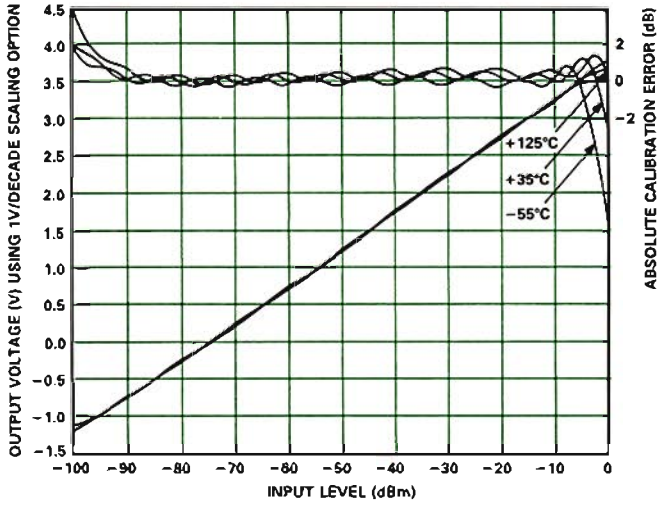


Figure 3. Output and error of cascaded AD640s over the range −100 dB to 0 dBm (square wave) at −55, +35, and +125°C.

gain; a log amp's large-signal gain, V_{out}/V_{in}, is of little practical significance. As Eq. 2 shows, the gain is proportional to V_y but—surprisingly—independent of the intercept voltage, V_x.

IMPLEMENTATION

At low frequencies, the reliable logarithmic relationship between the collector current and base-emitter voltage of a bipolar transistor can be used to realize a circuit having a logarithmic transfer function with adequate bandwidth. In high frequency applications, since the primary objective is usually to provide high gain for small signals, some form of a cascade of amplifier stages is used; but compression is also required at each stage to avoid saturation so as to continue to respond to increasingly large inputs. Also, for such signals as amplitude-modulated sinusoids, there must be identical response for either sign of V_{in}. The mathematical requirement that the argument in Eq. (1) must be positive for real signals should not be a cause for concern; practical circuits can be designed to perform equally well for inputs of either polarity.

The AD640's *progressive-compression* principle provides a function that is actually only an *approximation* to a logarithmic response (and not as mathematically satisfying as the transistor relationship), but the fit can be arbitrarily close. Such log-amps comprise a chain of identical stages, each having a well-defined gain for small signals—and diminished gain above a critical input amplitude. For very small signals the overall gain is high, because few of the stages have reached the diminished-gain point; but as the input increases, each stage in the chain successively reaches the critical amplitude, its gain drops to a lower value, its incremental contribution to the output decreases, thereby compressing the output.

A VIDEO LOG-AMP ANALYSIS

The example to be discussed here differs from the AD640 but may nevertheless be useful to an understanding of successive-compression principles. Its logarithmic output is just the final output of a cascade of voltage-amplification stages, rather than the sum of current outputs from amplifier-limiter stages (for a discussion of the latter type, see the footnote† on page 3).

Consider N cascaded stages, each having a small-signal gain (numerical ratio) of A, and a break-point voltage of E. Local input and output voltages are V_i and V_o respectively (to distinguish them from the end-to-end signals V_{in} and V_{out}). What happens above this breakpoint depends on the type of amplifier. In this simplified case, the gain drops to *unity*, hence it is a "*dual-gain*" amplifier (Figure 4). The output of the chain's final stage is approximately logarithmic in form. (In the AD640, a chain of *amplifier/limiter* stages is used and the outputs of all limiters are *summed* to form the logarithmic value. The principle is similar.)

A linear amplifier's fixed gain is a dimensionless quantity, but in a nonlinear system, one or more reference voltages are involved in *scaling* the function. The transfer function in Eq. (1) contains two fixed voltages, V_x and V_y, which determine the accuracy of the system. Their source in this example is the voltage, E, embedded in the dual-gain stage; both V_x and V_y are *proportional* to this voltage, as will be demonstrated.

The theory can be fully developed using a five-stage example, as shown in Figure 5. The labeling "$A/1$" in each of the amplifiers denotes a dual-gain element, having a gain of A for small inputs

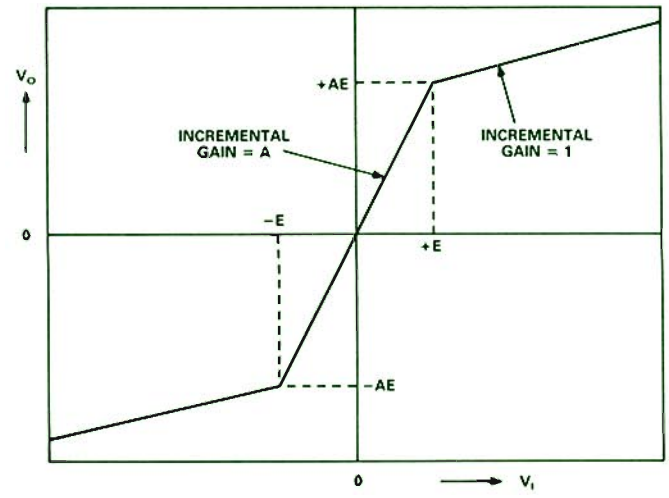


Figure 4. Input/output relationship for "dual-gain" amplifier.

and 1 for large inputs. We are concerned here only with the response of the system to its instantaneous input voltage. The dc transfer function of these elements is described by two equations:

$$V_o = AV_i \qquad \text{for } V_i < E$$
$$V_o = V_i + (A - 1)E \qquad \text{for } V_i > E \qquad (3)$$

For very small inputs, the overall gain is just A^N. Thus, for $A = 4$, the gain of the five cascaded amplifiers is 1,024. Shown beneath the amplifier chain are the inputs and outputs of these amplifiers at five critical input levels, identified as (a) through (e). The first (a) occurs when the input to the *last* stage is exactly E, at which point the system output is $V_{out} = AE$. (This critical input is called the "lin-log" transition; above it, the system begins to compress, while for smaller inputs it behaves as a linear amplifier). It must correspond to an input, $V_{in} = E/A^4$ (for five-stages, but E/A^{N-1} in general). The next critical point (b) occurs when the input to the *fourth* stage is E, corresponding to $V_{in} = E/A^3$, that is, at an input voltage A times larger. Meanwhile, V_{out} has increased from AE to $(2A - 1)E$, from Eq. (3); that is, it has increased by $(A - 1)E$. Continuing this process, we note that V_{out} increases by a constant *linear* amount $(A - 1)E$ for each *factor of* A increase in V_{in}.

Figure 6 is the calculated plot of V_{out} versus V_{in} (on linear scales) for the design choice $A = 4$ (about 12 dB) and $E = 50$ mV. It is apparent that compression is occurring on a quasi-logarithmic curve. For comparison, Figure 7 plots V_{out} on a linear scale versus V_{in} on a logarithmic one. The actual response shows a series of

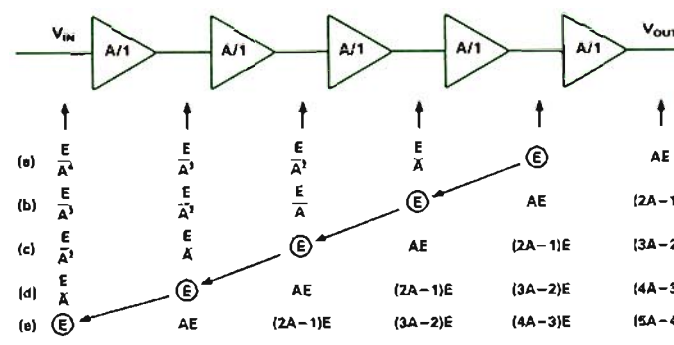


Figure 5. Cascaded dual-gain stages showing progressive compression as critical input is reached for each stage.

cusps, but the five transition points, (a) through (e), lie exactly on a line (dotted) representing the ideal logarithmic response, corresponding to Eq. (1).

Since a factor of 10 is 1 decade, "a factor of A" can be expressed as $\log_{10}A$ decades. For $A < 10$ (the usual case in a log-amp) the value will be fractional. Thus, a ratio of 4 is about 0.6 of a decade, because log(4) = 0.602. For $A = 3.162$ (i.e., 10 dB), the critical points are half a decade apart, and so on.

So the *slope* (of the dotted line in Figure 4) can be expressed as

$$\textit{Slope voltage} = V_y = \frac{(A-1)E}{\log A} \text{ (volts per decade)} \quad (4)$$

Eq. (4) predicts $V_y = 0.249$ volts per decade in this example.

Knowing V_y, we can solve for V_x by substitution in Eq. (1):

$$V_{out} = \frac{(A-1)E}{\log A} \log \frac{V_{in}}{V_x}$$

using, say, the input/output pair $V_{in} = E/A^4$, $V_{out} = AE$. The solution for V_x turns out to be

$$\textit{Intercept voltage} = V_x = \frac{E}{A^{5\,+\,1/(A\,-\,1)}} \quad (5)$$

(In general, "5"—in the exponent—would be replaced by the number of stages, N.) From Eq. (5), the intercept, V_x, for this example is 30.76 μV. The amplifier just described works equally well with positive or negative values of V_{in}.

ACCURATE BIASING THE KEY

The design of the AD640 is based on very simple amplifier/limiter stages; its parameters, such as gain and knee voltage (where each stage begins to limit) are well controlled for system predictability. The basic amplifier is nothing more than a bipolar long-tailed-pair, "LTP" or "diff-amp," which conceals more than a few pitfalls. For example, the differential small-signal gain, A, of an ideal LTP, having a tail current of I and two load resistors, R, is simply $A = R/r_e = qIR/(2kT)$. The most obvious design requirement, therefore, is that the tail current must be proportional to the absolute temperature, T. This is commonly referred to as "PTAT." That is just one of many details which must be carefully considered in taming the LTP.

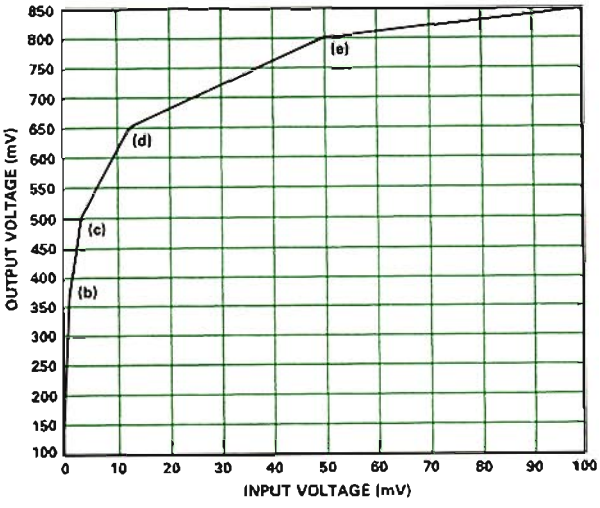


Figure 6. Output of last stage of system shown in Figure 5.

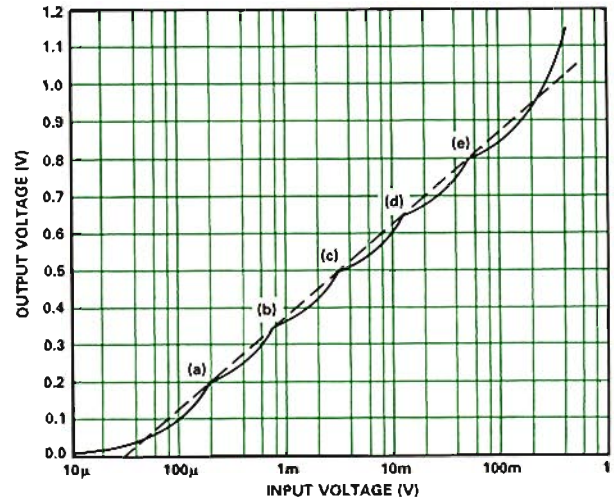


Figure 7. Transfer function of conceptual device using dual-gain, plotted on log-lin scales; the dotted line corresponds to the ideal logarithmic function of Eq. (1); compare Figure 3.

The AD640 resorts to precision biasing techniques to achieve its goals. Figure 2 shows that in addition to the amplifier/limiter stages (which are simple and exhibit very clean overload characteristics), there are three biasing blocks. One—the "gain regulator"—provides basically PTAT tail currents but introduces many small corrective terms for lot-to-lot production tolerances. This works well; gain comes out within a small fraction of a dB and is not trimmed. A second block—the "slope regulator"—performs a similar task in setting up the slope of the logarithmic function (see below). A third block—the "intercept positioning bias"—sets the intercept to an exact value and stabilizes it over temperature.

The primary reference for the slope and intercept is a bandgap circuit; it can be quite accurate using careful design and layout techniques, but the thin-film resistors have a lot-to-lot tolerance of several percent. The resistors that relate to the output-current calibration must therefore be trimmed to absolute value so that the outputs of any number of AD640s can be added by direct summing at a node, without the need for trimming by the user. Also trimmed are small residual errors such as input offset voltage (to instrumentation-amplifier levels of typically 50 μV).

TEMPERATURE STABILITY

Earlier, it was shown that the *scaling* of the slope and intercept of a log-amp ultimately depend on the knee voltage of the limiter stage. But for a simple LTP, this voltage is $2kT/q$, about 52 mV PTAT, a strong function of temperature! The solution is found in applying some basic nonlinear-analog-circuit principles. Figure 3 shows both the video output and the deviation of this output from the ideal transfer function, for two AD640s in cascade, using a low-frequency square-wave and with bandwidth restricted to 100 kHz. The superior scaling calibration and temperature stability of the AD640 result from our designing it from the outset as a high-speed nonlinear function circuit, rather than taking a traditional amplifier-design approach.

GROUNDING FOR LOW- AND HIGH-FREQUENCY CIRCUITS

Know Your Ground and Signal Paths for Effective Designs

Current Flow Seeks Path of Least Impedance—Not Just Resistance

by Paul Brokaw and Jeff Barrow

Noise reduction is a significant design issue in most electronic systems. Along with dissipation constraints, ambient temperature changes, size limitations, and speed & accuracy requirements, noise is an omnipresent factor that must be dealt with for a successful final design. We are not concerned here with techniques for reducing *external noise* (which arrives with the signal); since its presence is generally beyond the direct control of the design engineer; it must be dealt with in the operational design of the system by means such as filtering, analog signal processing, and digital algorithms.

In contrast, preventing *internal noise* (noise generated or coupled within the circuit or system) from corrupting the signal is a direct responsibility of the design engineer. Noise sources, if not fully considered *early in the design cycle*, can adversely affect final performance and prevent the high-resolution potential of a system from being realized; at the very least, costly redesign and rework may be required. Some of the design factors that relate noise to system behavior have been treated in earlier articles in these pages[1,2,3,4,5]. Here, we consider the major role that schematic, topology, and final layout of the system "ground" play in minimizing the coupling of internally generated noise.

To deal adequately with noise, we need several perspectives: the actual internal pin connections of a component, versus the conceptual ones; the proposed schematic for ground-referenced signals; and the effects of layout on noise generation and pickup. These subjects divide into two overlapping domains, depending on bandwidth of the noise phenomena; ground-noise sources, problems, and solutions differ at low and high frequencies. Fortunately, good grounding practices in one band are generally compatible with those in the other.

BASIC OP-AMP INTERCONNECTIONS

Many discussions of op amps present the ideal op amp as a three-terminal device with a pair of differential inputs and a single output (Figure 1). But the output voltage has to be measured with respect to some reference point, and output current from the amplifier must find a closed circuit back to the amplifier. The infinite common-mode rejection of the ideal differential op amp disengages the input and output reference potentials, and the high input impedance eliminates the possibility of using an input terminal as an output current return; so there must be a fourth terminal, which some call "ground."

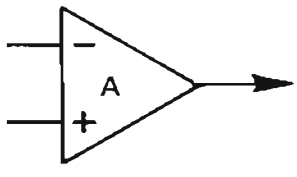


Figure 1. Conventional "three terminal" op amp.

Of course, most IC op amps don't have a "ground" connection; the fourth terminal is generally considered to be the common connection of a dual power supply (which may also be serving other amplifiers and system elements). While it indeed serves this function at low frequencies, it will continue to do so only as long as the supply connections actually present the amplifier with a low (ideally zero) impedance at all frequencies within the amplifier bandwidth. When this requirement is not met, the impedance at the supply terminals affects the signal path and a wide variety of problems will arise, including noise, poor transient response, and oscillation.

An op amp must accept a fully differential signal and convert this to a single-ended output, with respect to the fourth terminal. Figure 2 shows the actual signal flow used by several basic and popular op amp families. Most of the voltage difference between the amplifier output and the negative rail appears across the compensating capacitor of the integrator (which controls the open-loop frequency response); if the negative supply voltage changes abruptly, the output of the integrator amplifier will immediately follow its "+" input. With the op amp in a typical closed-loop configuration, the input error signal tends to restore the output, with recovery limited by the integrator bandwidth.

This type of amplifier may have excellent low-frequency power-supply rejection, but negative supply rejection is limited at higher frequencies. Since the amplifier's gain is what causes the output to be restored, the negative supply rejection approaches zero for signals above the closed-loop bandwidth. The result: high-speed, high-level circuits can interact with the low-level circuits through the common impedance of the negative supply line.

Decoupling often is the recommended solution, but there are many wrong and some better ways. A decoupling capacitor *near the*

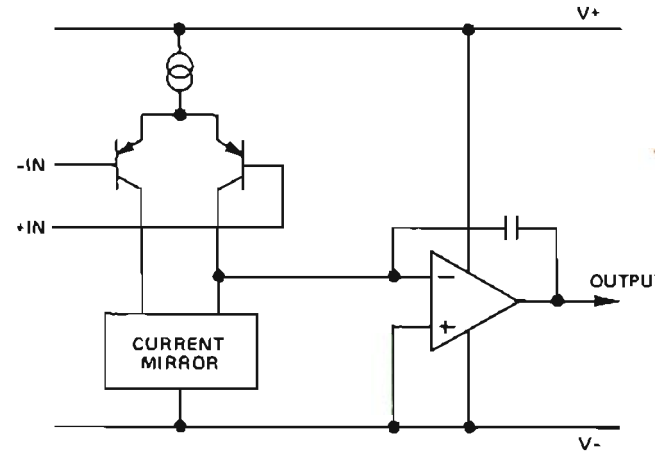


Figure 2. Simplified "real" op amp.

[1] "Noise and Operational Amplifier Circuits," by D. H. Sheingold and L. R. Smith, *Analog Dialogue* 3-1 (1969).
[2] "Understanding Interference-Type Noise," by Alan Rich, *Analog Dialogue* 16-3 (1982).
[3] "Shielding and Guarding," by Alan Rich, *Analog Dialogue* 17-1 (1983).
[4] "Ground Rules for High-Speed Circuits," by Don Brockman and Arnold Williams, *Analog Dialogue* 17-3 (1983).
[5] "Amplifier Noise Basics Revisited," by Al Ryan and Tim Scranton, *Analog Dialogue* 18-1 (1984).

power supply may be separated from the op amp by many centimeters of wire, which looks like a high-Q inductor. Placing the decoupling capacitor near the op amp may still not solve the problem since, for decoupling, the other end of the capacitor must be connected to that mystical somewhere called "ground."

Figure 3* shows how a decoupling capacitor is connected to to minimize disturbances between the negative rail and ground buses. The load current's high-frequency component is confined to a path that doesn't include any part of the ground path. As an example of a more complex case, in Figure 4, the op amp is driving a load that goes to virtual ground (input of the second amplifier) and actual load current does not return to ground. Instead, it must be supplied by the second amplifier via its positive supply. Decoupling the negative supply of the first amplifier to the positive supply of the second one closes the high-speed signal current loop without affecting ground or signal paths.

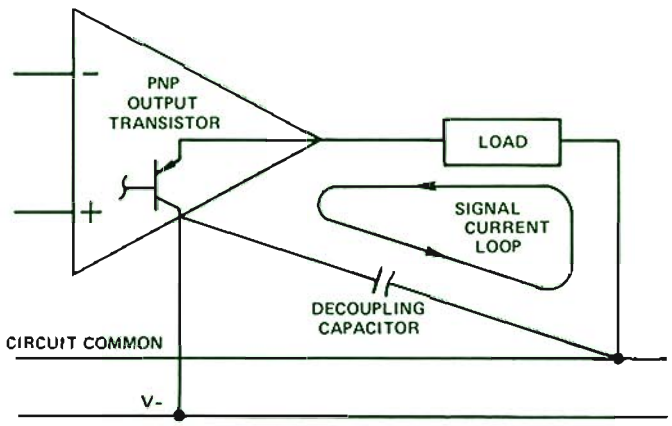


Figure 3. Decoupling of negative supply for a grounded load.

Allowing ground currents to share a path with a low-level signal can cause problems. Figure 5 shows how careless grounding can degrade the performance of an amplifier driving a load resistor. The load current is supplied by the power supply and controlled by the amplifier. If points A and B are power supply "ground" connections, connecting the supply at A causes the load current to share a segment of wire with the input signal connections.

For example, fifteen centimeters of number 22 wire present about 8 mΩ of resistance to the load current. For a 2-kΩ load, a 10-volt

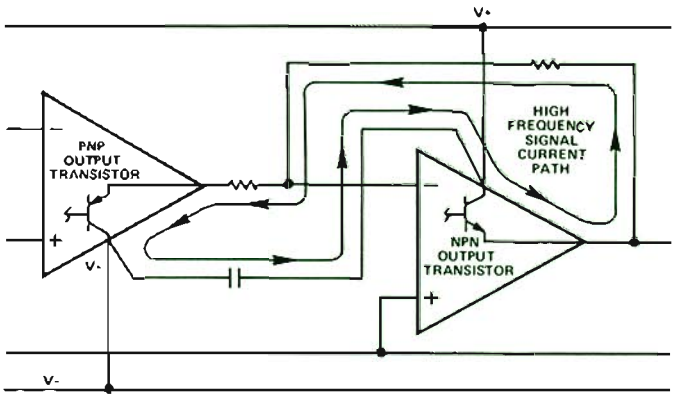


Figure 4. Decoupling of negative supply for "virtual ground" load.

*Many of these illustrations can be found in the free Application Note, "An I. C. Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by Paul Brokaw.

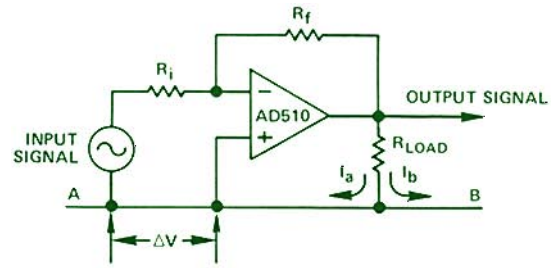


Figure 5. Proper choice of power connections will minimize this problem.

output swing results in about 40 μV between the points marked ΔV. This signal is in series with the non-inverting input and can result in significant errors: for an amplifier with a gain of 8 million, this positive feedback of 1/250,000 introduces a gain error factor 32× worse than that associated with the amplifier's open-loop gain alone. In addition, the positive feedback can cause circuit latchup or oscillation for large closed-loop gains (typically >250 V/mV). But the common feedback impedance can be eliminated by connecting the power supply to point B.

In a real system, the situation is more complicated. The input signal source, shown as floating in Figure 5, may also produce a current which must be returned to the power supply. With the supply's return at B, any current flowing in additional loads other than R_i may interfere with this amplifier's operation. Where amplifiers are cascaded, the scheme in Figure 6 shows how they can still drive auxiliary loads without common-impedance feedback coupling. Output currents flow through auxiliary loads and back to the power supply through the power common. Bypasses

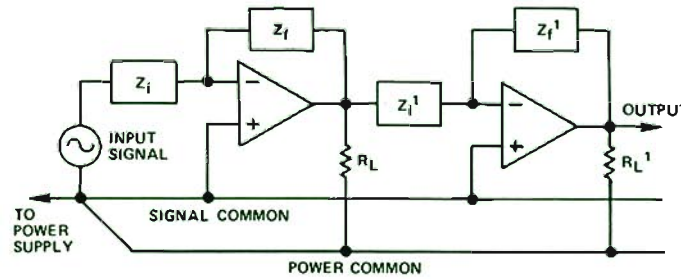


Figure 6. Minimizing common impedance coupling.

are connected as shown in Figure 4 so that currents in the input and feedback resistors are supplied from the power supply via the amplifiers. Only amplifier input current flows in signal common; its effect is usually small enough to ignore.

Understanding where the actual load and signal currents go is essential. The key to optimizing the circuit is to bypass these currents around ground and other signal paths. The voltage —more accurately called the potential difference—between two points defines such a current flow.

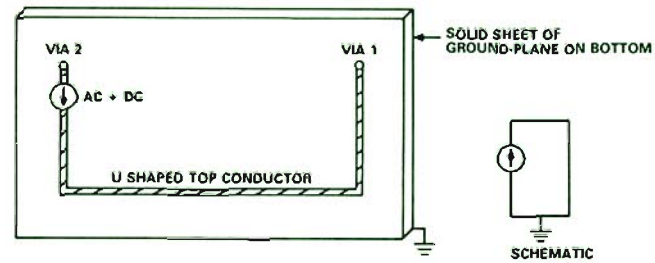


Figure 7. Schematic and layout of current source with U-shaped trace on pc board and return through ground plane.

GROUNDING FOR HIGH-FREQUENCY OPERATION

The "ground-plane" layer is often advocated as the best return for power and signal current, while providing a reference node for converters, references, and other subcircuits. However, even extensive use of a ground plane does not ensure a high quality ground reference for ac circuits.

The simple circuit shown in Figure 7, built on a two-layer printed circuit board, has an ac and dc current source on the top layer connected to via 1 at one end and to a single U-shaped copper trace connected to via 2. Both vias go through the circuit board and connect to the ground plane. Ideally, impedance is zero and the voltage appearing across the current source should be zero.

The simple schematic hardly begins to show the actual subtleties. But an understanding of how the current flows in the ground plane from via 1 to via 2 makes the realities apparent and shows how ground noise in high-frequency layouts can be avoided.

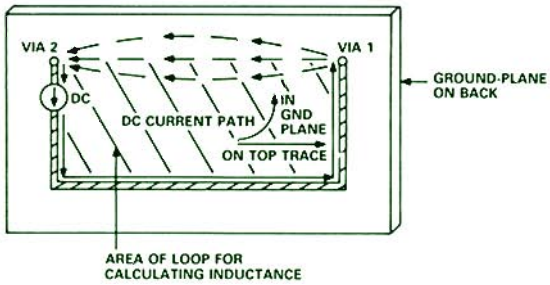


Figure 8. DC current path for Figure 7.

The dc current flows in the manner of Figure 8, as one might surmise, taking the path of least resistance from via 1 to via 2. Some current spreading occurs, but little current flows at substantial distance from this path. In contrast, the ac current does not take the path of least resistance; it takes the path of least *impedance*, which in turn depends on *inductance*.

Inductance is proportional to the area of the loop made by the current flow; the relationship can be illustrated by the right-hand rule and magnetic fields shown in Figure 9. Inside the loop, current along all parts of the loop produces magnetic field lines that add constructively. Away from the loop, however, field lines from different parts add destructively; thus the field is confined principally within the loop. A larger loop has greater inductance; this means that, for a given current level, it has more stored magnetic energy (Li^2), *greater impedance—since* $X_L = j\omega L$, and hence will develop more voltage at a given frequency.

Which path will the current choose in the ground plane? Naturally the lowest-impedance path. Considering the loop formed by the U-shaped surface lead and the ground plane, and neglecting resistance, high-frequency ac current will follow the path with the least inductance, hence the least area.

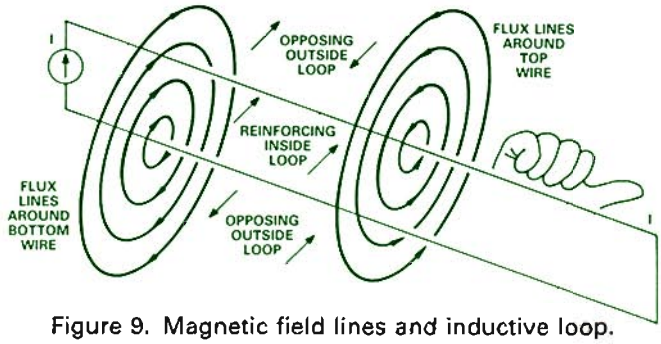


Figure 9. Magnetic field lines and inductive loop.

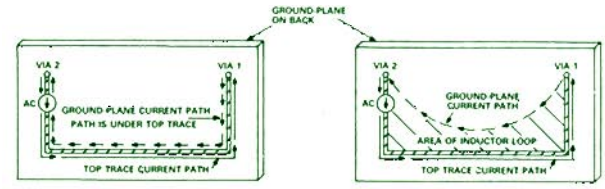


Figure 10. AC current path without (left) and with (right) resistance in ground plane.

In the simple example shown, the loop with the least area is quite evidently formed by the U-shaped top trace and the portion of the ground plane *directly underneath it*. So, while Figure 8 shows the dc current path, Figure 10 (left) shows that the path that most of the ac current takes in the ground plane, where it finds minimum area, directly under the U-shaped top conductor. In practice, the resistance in the ground plane causes the current flow at low- and mid-frequencies to be somewhere between straight back and directly under the top conductor (right). However, the return path is nearly under the top trace even at frequencies as low as 1 or 2 MHz.

Avoiding Layout Problems Once the return current paths in the ground-plane are understood, common layout trouble spots can be identified and corrected. For example, in Figure 11, path A is identified as critical, to be kept short, away from digital lines, and free of vias. Path B is of lesser importance, but needs to cross A. Typically, the ground plane is cut under A, and B is then routed through two vias and under A.

The unfortunate result is that inductance is introduced into the ground returns of both signals, because the interrupted ground plane makes both return loops larger. Since path A conducts a high-frequency signal, an induced voltage drop will appear across the opening of the ground plane. For typical ECL or TTL signals, this drop can be greater than several hundred millivolts, enough to seriously compromise the performance of a 12-bit, 10-MHz converter or an 8-bit, 20-MHz unit. A simple fix is to install a wire directly across the cut in the ground plane to keep the loop area small.

Power distribution is another area of concern. Power supply lines must be kept at lowest possible characteristic impedance ($\sqrt{L/C}$). To keep this ratio small, inductance is reduced and capacitance increased by maintaining ground planes under the supply lines; capacitance can be further increased by selectively placing bypass capacitors at critical locations, as discussed earlier. If only capacitance is dealt with by, for example, placing 0.1-μF capacitors on supply pins to lower their impedance, a supply line with 30-nH inductance will have damped oscillations at about 3 MHz after every transient. ◘

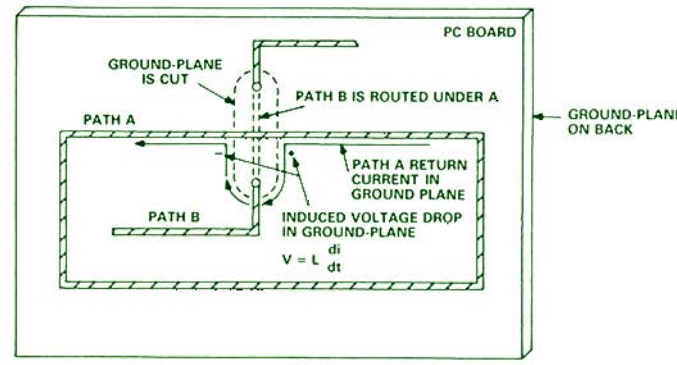


Figure 11. Typical PC layout problem, with paths crossing.

8-BIT FLASH A/D CONVERTERS ENCODE AT UP TO 300 MSPS

AD9028/AD9038 Have 47-dB SNR at 9.3 MHz and 250 MSPS

Demultiplexed AD9038 Can Feed Alternate Samples to 2 Databanks

by David Duff

The AD9028 and AD9038, ECL-compatible 8-bit flash analog-to-digital converters* with 250-MHz large-signal bandwidth, can encode at up to 300 MSPS. An advanced bipolar process provides superior ac linearity and dynamic range; and these monolithic devices need just a single −5.2-volt power supply.

The two devices are essentially identical—with one difference: The AD9028 provides conversion data via a single output port, while the AD9038 is a 1:2 "demultiplexed" version, which alternately places output bytes on two ports. Although the single-port approach is more straightforward in concept, the deMUX scheme allows slower memories or logic to be used; they see an effective data rate of one-half the encode rate. When converting at rates in the neighborhood of 300 MSPS, a 150-MHz memory update rate can mean significant cost savings.

Analog Inputs The specified peak-to-peak analog input range is 0 to −2.0 V. Input capacitance is less than 17 pF; and it can be reduced by biasing the collectors of the input transistors via an Analog Return pin. When the collectors are connected to ground, the collector-base capacitance causes the analog input capacitance (as seen by the source) to vary with the input voltage. The signal must come from a low-impedance source to drive this capacitive load adequately at the higher frequencies; where the drive is insufficient, distortion (mainly second-harmonic) results.

When the Analog Return is connected to a dc voltage between ground and +1.5 V, the ac performance is improved (Figure 2), by reducing the input capacitance and its dependence on the analog input voltage. The capacitance, and its variations, can be further reduced if the analog return is driven by a level-shifted and buffered version of the analog input signal in the manner of a

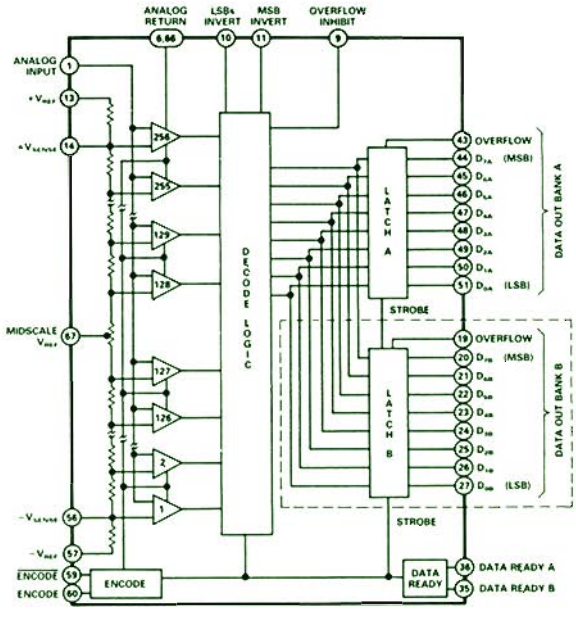
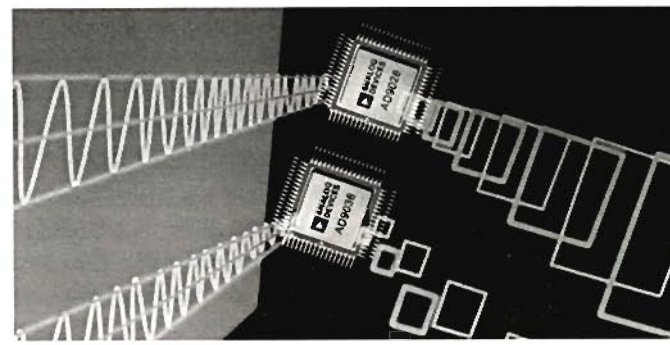


Figure 1. AD9038 functional block diagram. The AD9028 is similar but omits the dashed area.

*Use the reply card for technical data.



driven guard, biased up by about +1 V. Although a low-distortion, low-noise amplifier with wide bandwidth and superior ac characteristics is required, it need not have high dc accuracy.

User-supplied references for this converter are normally set at 0 and −2 V. *Sense* pins at the reference contacts allow calibration of the full-scale range; and a midpoint tap of the reference ladder can be used to adjust integral nonlinearity via external resistors.

Digital Outputs: Data outputs are presented as ECL-compatible signals. The single-port AD9028 has a Data-Ready signal; the two-port AD9038 has a Data Ready signal for each port. Two control lines, MSB Invert and LSBs Invert, permit any combination of senses for the *most-* and *less-*significant bits; this permits four output formats: binary, twos complement, and their inverses. In addition, an Overflow-Inhibit pin set by the user determines the state of the overflow and digital output bits when the input exceeds $+V_{SENSE}$.

Performance: The AD9028 and AD9038 have many guaranteed- and tested specifications. For example, typical signal-to-noise is 36 dB (33 minimum) for a 92-MHz input and 47 dB (45.5 min) for a 9.3-MHz input, tested at 250 MSPS. Harmonic distortion products are −40 dBc (−36 min) and −56 dBc (−54 min) at the same frequencies. Typical power dissipation is 2.1 W. Available packages, designed for low thermal impedance, are 68-pin leaded and leadless ceramic chip carriers. Prices start at $185 (100s).

The AD9028 and AD9038 were designed by Tom Tice at Analog Devices' Computer Labs Division, Greensboro, North Carolina.

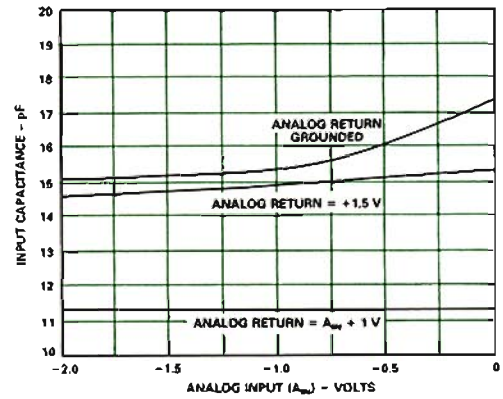


Figure 2. Reduction of input capacitance with driven analog return.

22-BIT A/D-CONVERTER EVALUATION BOARD FOR THE PC

AC5005 Transforms IBM PC/XT/AT into a 6 1/2-Digit Voltmeter

Eliminates the Need for Breadboards and Test Programs

by Bill Sheppard

The AC5005* is an IBM PC/XT/AT-based evaluation board for Analog Devices' AD1175K, a 22-bit multi-slope integrating analog-to-digital converter. The AC5005 quickly and easily evaluates the AD1175K. The combination forms a powerful computer-based high-resolution data-acquisition system.

The AD1175K (*Analog Dialogue* 21-2, pp. 9-11) is industry's most accurate *complete* 22-bit analog-to-digital converter. μP-based, its proprietary autozeroed, multi-slope integration technique achieves high accuracy and low noise, with ±$^1/_2$-LSB max 22-bit differential nonlinearity (DNL) and ±$^1/_2$-ppm max integral nonlinearity (INL) at an impressive 20 conversions per second.

Engineers developing ultra-high-resolution data-acquisition systems face major challenges. First they must find high-precision, cost-efficient hardware. Then—a more-difficult task—evaluate and implement the hardware in the target system. The AC5005/AD1175 pair and an IBM PC/XT/AT provide the necessary hardware and software tools to get the job done. The AC5005 comes with schematics, assembly drawings and a sample BASIC program. Besides demonstrating good design practices for users to follow in PC-board layout, it can be used as an example for practically any interface-board bus structure.

Plugged directly into a slot of the IBM PC/XT/AT backplane, the AD1175K/AC5005 demonstrates its full 22-bit resolution in a harsh, noisy environment; the backplane's bus has noisy switchers, high-frequency clocks, and heavy digital traffic.

The AC5005 comes with menu-driven demonstration software

that exercises all eight of the AD1175K's functions and emulates a 6-1/2 digit DVM. The on-board multiplexer allows selection of four differential analog input channels via software. Ten digital I/O lines are available to the user to control lamps and actuators, as well as to test switch positions. The end-to-end gold plating on the AC5005 analog input connector's pins effectively eliminates errors due to thermocouple effects. Analog circuit power is supplied by ADI's workhorse model 940 dc-to-dc converter. A user-configurable jumper sets the AD1175K's integration time for a multiple of the line frequency to maximize rejection of 60- or 50-Hz noise at 20- or 16 conversions per second.

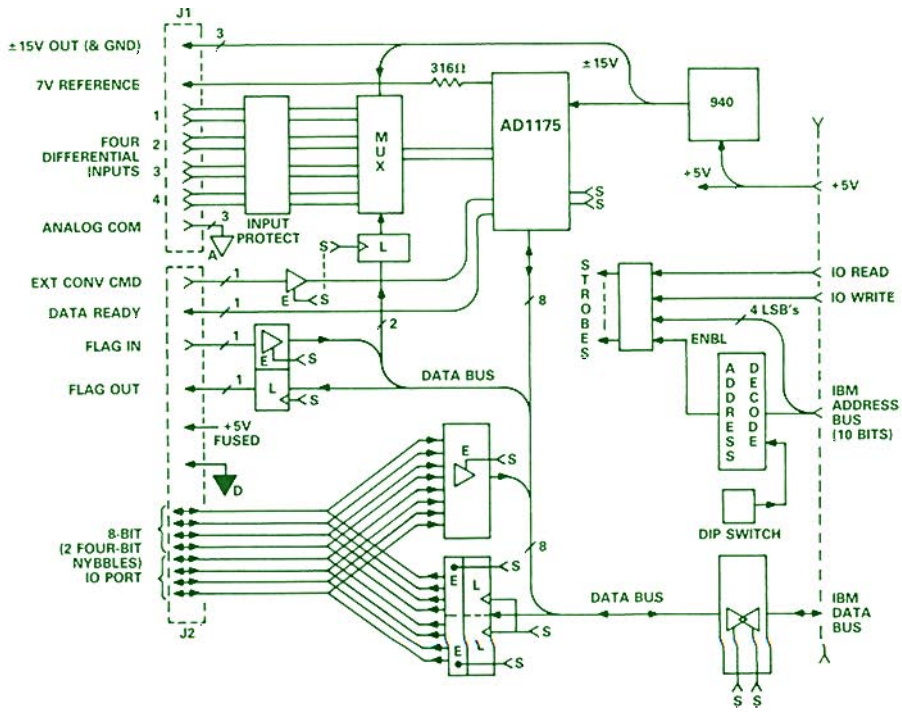


Figure 1. AC5005 block diagram.

The AC5005/AD1175K turn an ordinary PC into a low cost 6$^1/_2$-digit voltmeter or measurement and data-acquisition system, with ultra-high accuracy (0.12 ppm max DNL and 0.5 ppm max INL). This performance has been achieved using an ordinary twisted pair of wires on the input. The combination is suitable as an integral part of test and measurement equipment in the laboratory, on the factory floor, or used in portable PCs for the field. Applications include instrumentation (chromatography, spectroscopy, seismology, etc.) and weighing systems.

The AC5005 is specified for 0 to +70°C operation. Price of the AD1175K is only $495 in 100s ($795 for singles); the AC5005 evaluation board is priced at $495 (1's).

The AD1175K and AC5005 were designed by Geoff Haigh at Analog Devices' Industrial Products Division, Norwood, Massachusetts.

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14-BIT, 100 kSPS MONOLITHIC SAMPLING A/D CONVERTERS

1 MHz Full-Power and 500-kHz Full-Linear Bandwidth, 80-dB SNR

AD1779 for 16-Bit Bus, Two-Byte AD1679 for 8-Bit Bus

The AD1679 and AD1779* are ADI's first monolithic 14-bit sampling analog-to-digital converters. Complete on a single BiCMOS chip, each includes a recursive-subranging ADC, sample-hold amplifier (SHA), precision voltage reference, clock, and processor interface. They are identical, except that the AD1779 interfaces with a 16-bit (or wider) data bus in a single *read* operation, while the AD1679 feeds two bytes (8 + 6) onto an 8-bit bus (Figure 1).

Designed, specified, and tested for signal-processing applications, these devices feature 1-MHz *full power* bandwidth (−3 dB) and 500-kHz minimum *full-linear* bandwidth (i.e., the frequency at which the slewing rate of the sample-hold has been reached and the amplitude of the reconstructed fundamental is flat to within 0.1 dB).

Signal to noise-plus-distortion—S/(N+D)—is better than 80 dB (K grade) for 100 kSPS sampling of 10.009 kHz signals; it is significantly reduced only at much higher signal frequencies (Figure 2). *Total harmonic distortion is* −84 dB maximum, as is *intermodulation distortion*.

Many on-chip features greatly simplify circuit design and save board space by merging all the traditional support components onto a single IC. For example, the devices' 10-MΩ input impedance eliminates the need for a powerful source driver or an external buffer amplifier. The wide bandwidth specifications permit the devices to handle a broad range of input signals; filters used ahead of an ADC can be specified in confidence that the converter does not degrade system performance by introducing additional filtering. In addition, signals can be undersampled far beyond the Nyquist frequency of 50 kHz, attractive for applications capturing information from a high-frequency carrier.

The complete digital interface permits a microprocessor or a digital signal-processor to read the data in a choice of 8+6-bit format for 8-bit buses (AD1679), or as parallel 14-bit data for 16-bit, and wider, buses (AD1779). The AD1679 can operate in either a synchronous mode—under the direct control of a processor—or in an asynchronous mode, where it converts input signals independently of the processor—useful where conversion starts must be

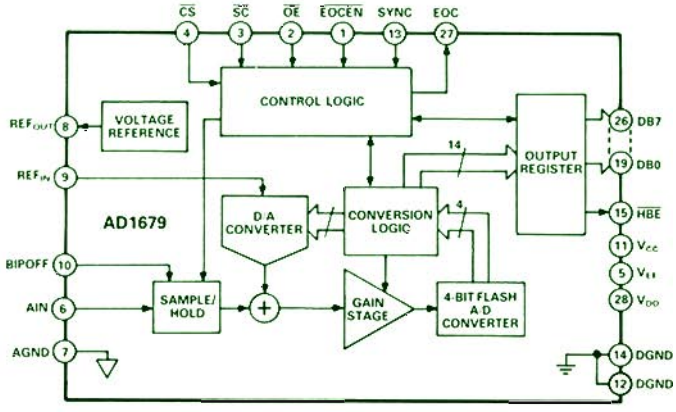

Figure 1. Block diagram of the AD1679.

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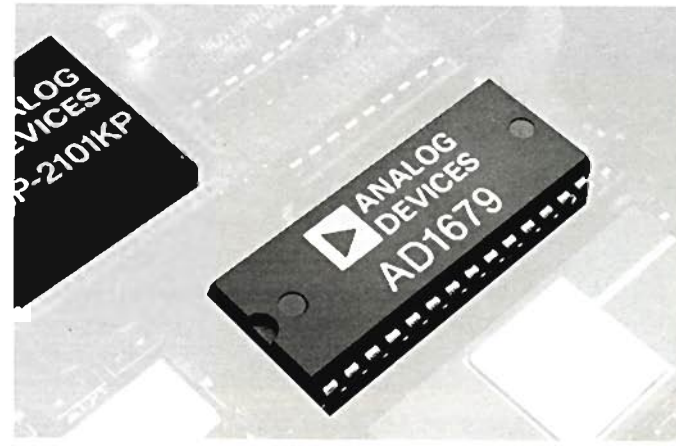


precisely timed. The AD1779 is asynchronous only. Maximum data-access time is 100 ns.

The AD1679 and AD1779 encode unipolar 0 to +10-volt input signals in straight binary and bipolar ±5-volt signals in twos complement. Required power supplies are ±12 volts and +5 volts; typical dissipation is 560 mW. The AD1679 is pin-compatible with the *12-bit* Analog Devices AD1678* (*Analog Dialogue* 23-1, pages 12-13); this permits system performance to be upgraded with little if any hardware redesign.

Each ADC is available in two grades, specified over the 0 to +70°C temperature range. Both the K and J grades have identical specifications, except for minimum S/(N+D): 80 dB and 78 dB. Because most ac signal-processing applications are insensitive to dc error sources, the AD1679 and AD1779 specify only "typical" dc parameters. However, both grades guarantee "no missing codes" over the specified operating temperature range.

Packaging options include 28-pin ceramic and plastic DIPs. Prices (100s) start at $39 (JN grade) and $43 (KN).

The design team for this converter family includes John Fernandes, Stephen R. Lewis, Martin Mallinson, Gerald A. Miller, and Larry Singer, of Analog Devices Semiconductor, Wilmington, MA.

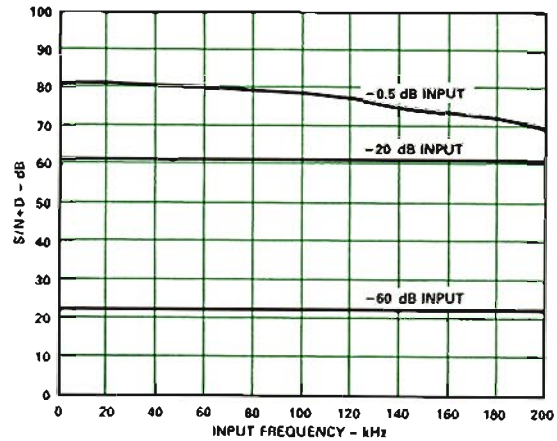


Figure 2. Signal to noise-plus-distortion as a function of input frequency and amplitude for 100-kSPS sampling.

A PAIR OF 16-BIT-PERFORMANCE SAMPLE-HOLD AMPLIFIERS

AD386 & AD1154: Designed for High-Performance Data Acquisition

AD386 for Speed & Temp Range; AD1154 for Size & Economy

by Pete Predella

The AD1154* and AD386* are sample-and-hold amplifiers (SHAs) designed for use with high-resolution analog-to-digital converters. Complete with internal Hold capacitor and proprietary error-compensation circuitry, these SHAs guarantee 16-bit accuracy. In addition, they are superior in speed and dynamic performance to many commonly used sample-holds in 14-bit high-speed data-acquisition and strobed measurement systems. Although their specs are somewhat similar (see Table), there are significant differences in size, price, input bandwidth and rated temperatures. The AD386 offers wider bandwidth and ranges of temperature; the AD1154 has a small package and a low price.

Output Polarity: Unlike many SHAs, the unity-gain AD1154 (Figure 1) is a noninverting type with a high-impedance (10^{12} Ω) analog input. Thus the output is unchanged in amplitude or polarity and there's no need to externally buffer the input.

The AD386's inverting architecture, on the other hand, produces a gain of −1 V/V. But an internal uncommitted unity-gain *difference amplifier* (Figure 2) can restore the signal's original polarity, with about the same input impedance—while also buffering ground.

Many data acquisition applications require distance between the SHA & converter and the signal source. It's not unusual to experience potential differences—between the source ground and the a/d converter—that affect measurement accuracy adversely. In such instances, shielded twisted-pair cable can be used to connect the remote source ground and signal to the AD386's differential amplifier. This technique will null most of the unwanted noise, reduce measurement errors, and enhance overall system integrity.

Feedthrough: Feedthrough is a residue of the ac input that appears at the output while in *hold* mode. It's caused by stray capacitive coupling from the input to the storage capacitor, principally across an open switch. Both SHAs achieve high feedthrough rejection through innovative circuit design and careful layout.

Temperature Options: The AD1154 is specified for the standard industrial temperature range, −25 to +85°C; the AD386 has B and T versions operating over extended-industrial and military operating temperature ranges of −40 to +85°C, and −55 to +125°C. The AD386T is available screened to MIL-STD-883B.

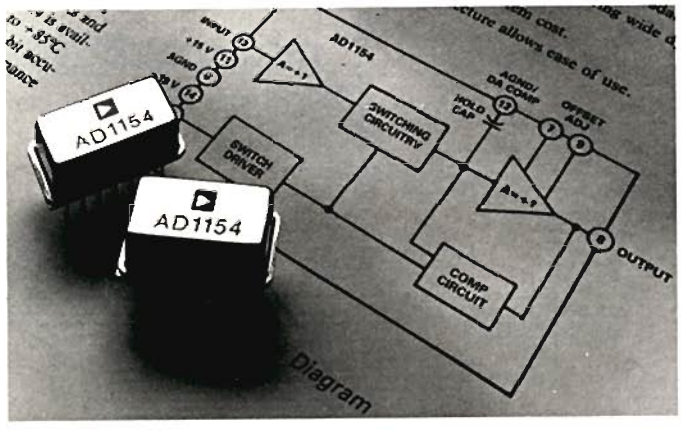


Figure 1. Block diagram of the AD1154.

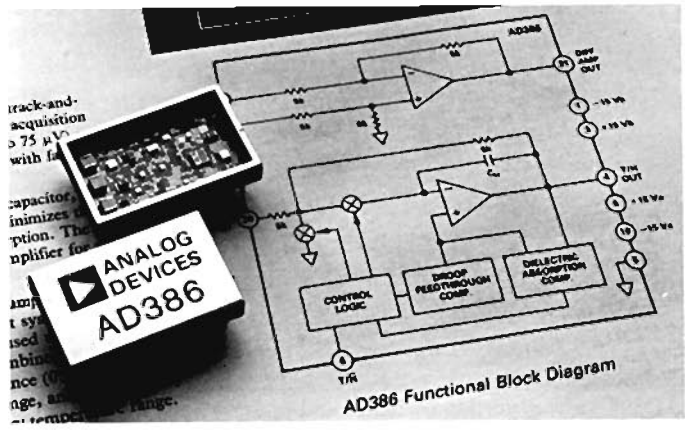


Figure 2. Block diagram of the AD386.

Packaged in a 14-pin metal DIP, the hybrid AD1154 is available in two grades, A and B, with ±0.0015% and ±0.00076% maximum *hold*-mode nonlinearity. Prices in 100s are $42 and $49.50, for the A and B versions.

The AD386 is housed in a 24-pin double-width ceramic DIP. B and T-grade prices (in 100s) are $79 and $99, respectively.

SPECIFICATION	AD1154AW/BW	AD386BD/TD
ANALOG INPUT/GAIN ACCURACY		
Voltage Range (V)	±10	±10
Input Impedance (Ω)	10^{12}	5 k
Gain (V/V)	+1	−1
Gain Error (max)	0.01%	0.02%
NONLINEARITY		
Sample Mode (max)	±0.0015% typ	±0.00076%/±0.003%
Hold Mode (max)	±0.0015%/±0.00076%	no spec
DYNAMIC SPECIFICATIONS		
Small Signal BW (−3 dB, MHz)	1	2
Noise (dc to 1 MHz, μV rms)	40	45 max
SAMPLE-TO-HOLD SWITCHING		
Aperture Delay (ns)	80	12
Aperture Jitter (ps)	150	40
Switching Transient		
Settling to ±0.003% (μs)	0.4	0.5 max
Settling to ±0.00076% (μs)	1	0.8
HOLD-MODE DYNAMICS		
Droop Rate (μV/μs) max	0.1/0.05	0.1
Droop Rate @ T_{max} (μV/μs) max	1	1/10
20-V p-p, 10-kHz Feedthrough, max	−96 dB	−94 dB (50 kHz)
HOLD-TO-TRACK SWITCHING		
Acquisition Time		
To ±0.003% of 20 V (μs max)	no spec	3.6
To ±0.00076% of 20 V (μs max)	8/5	4.5
TEMPERATURE RANGE		
Rated Performance (°C)	−25 to +85	−40 to +85/−55 to +125
PACKAGE	14-pin metal DIP	24-pin 2×wide Ceramic DIP
PRICE (100s)	$42/$49.50	$79/$99

The AD386 was designed by Steve Goldstein at Analog Devices' Microelectronics Division, in Wilmington MA; the AD1154 was designed by Tony Marino, at ADI's Industrial Products Division, in Norwood MA. ◘

*Use the reply card for technical data.

IC LVDT CONDITIONER IS INSENSITIVE TO USUAL ERROR SOURCES

Monolithic AD598 Is Complete: Oscillator, Reference, Ratiometric Decoders Operates from Single or Dual Supply; Output Is Unipolar or Bipolar

Linear variable-differential transformers—LVDTs—and their rotary counterparts, RVDTs, are widely used for position measurement in industry and aerospace because of their ruggedness, accuracy, and repeatability. The AD598* offers a complete monolithic signal-conditioning solution in a 20-pin package for interfacing them to systems. It has a primary oscillator for the LVDT—plus secondary decoding circuitry. Its output is a dc voltage proportional to the LVDT core position.

Fully trimmed and easy to apply, the AD598 needs no adjustments and requires few external components to set the desired frequency and gain. It is insensitive to transducer null voltage and primary-to-secondary phase shifts.

Internal functions are shown in the block diagram, Figure 1. The AD598's low-distortion oscillator and power amplifier (THD typically below −50 dB) drive the LVDT primary differentially with up to 24 V rms. A single capacitor sets oscillator frequency from 20 Hz to 20 kHz, and a resistor sets its output amplitude.

LVDT secondary outputs[1] consist of a pair of sine waves whose difference is proportional to the core position. In many traditional LVDT decoding circuits, the absolute value of the amplitude difference produces a voltage proportional to position. With this technique, high accuracy & stability require excitation at constant amplitude and frequency, with stable primary-to-secondary phase shift—hard to achieve with long leads, temperature changes, and varying excitation frequency. The phase-difference compensation must be readjusted when phase changes. Such problems impose constraints on the LVDT's physical relationship to the system.

The decoding circuitry of the AD598 uses ratiometric principles and implicit analog computation for a computed result that is insensitive to primary frequency or phase. The decoder, shown in Figure 2, uses signal differences, an integrator, a comparator, and multiplication by a continuously adjusted duty cycle to produce a ratiometric current, $(A - B)/(A + B)$ times the internal current reference, where A and B are the secondary signals. Filtering and buffering provide the final output voltage.

The approach's advantage is that *transducer null voltage*, the nonzero LVDT output at the mechanical null position—and primary-to-secondary phase shifts, difficult-to-deal-with sources of error

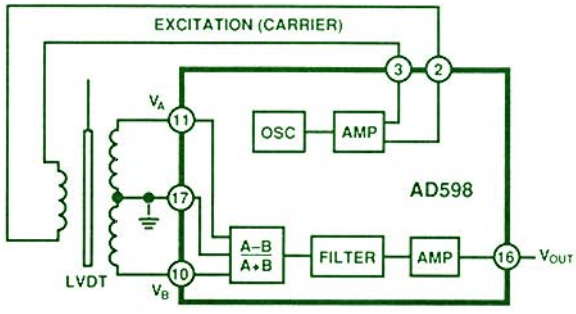
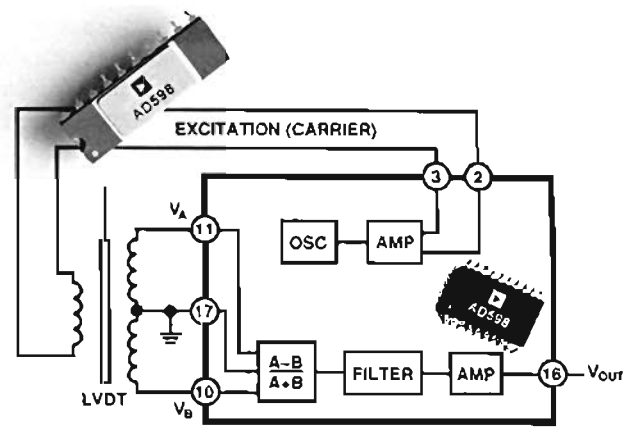


Figure 1. Functional block diagram.

*Patent pending. Use the reply card for technical data.

[1]See "The Easy Way to Interface an LVDT to Digital," *Analog Dialogue* 20-2, 1986 (pages 19-21).



and instability associated with traditional LVDT interfaces—do not affect accuracy. The LVDT can be hundreds of feet away from the AD598 with no performance degradation, useful where system electronics should be kept away from an LVDT's harsh environment. For remote data applications, the AD598 decoder output buffer can drive up to 1,000 feet of cable.

Since no lead-wire compensation is required, LVDT units are interchangeable, another user advantage. Multiple LVDTs (series or parallel) can be driven from one of the AD598s (within power limits) since the oscillators of the other AD598s are not involved in the decoding; an *external* power oscillator can be used in multichannel applications such as simultaneous gaging systems.

The AD598 is linear to within 100 ppm. Its output voltage can be either unipolar or bipolar, operating from unipolar or dual supplies. For example, its output range is ±10 volts with dual supplies as low as ±12 V; it will operate with one-sided supplies of beyond 30 volts. Gain- and offset drift specs are 50- and 20 ppm/°C. The AD598 is available in a 20-pin small-outline (SOIC) or a side-brazed ceramic DIP. Price begins at $13.95 in 100s.

The AD598 was designed by Larry DeVito of the Analog Devices Semiconductor division of ADI, Wilmington, Massachusetts.

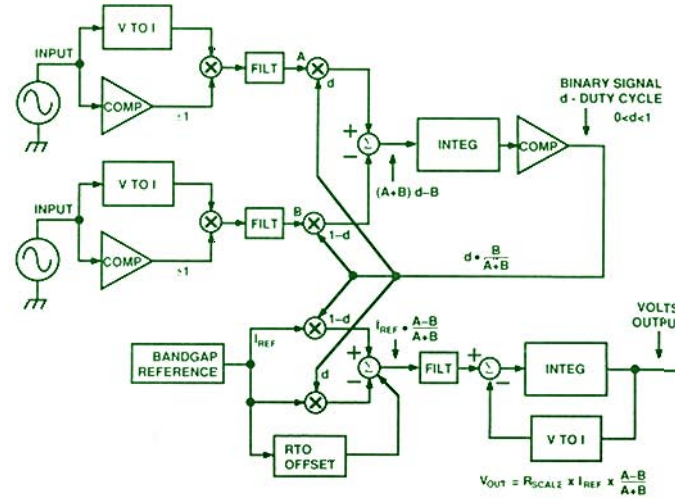


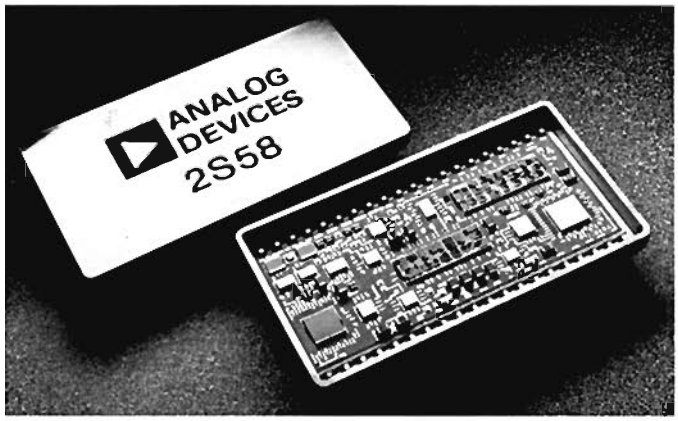
Figure 2. Decoder block diagram.

RATIOMETRIC 16-BIT LVDT-TO-DIGITAL CONVERTER

2S58 Ignores Changes in Excitation Voltage, Frequency, & Waveshape
Has < 0.01% Nonlinearity, 1-LSB Repeatability, 10 to 50 V/V Gain

The 16-bit Analog Devices 2S58* is the newest member of a proven family of data converters for linear variable differential transformers (LVDTs) and their rotary version, RVDTs—first introduced in these pages in 1986 ("The Easy Way to Interface an LVDT to Digital," *Analog Dialogue* 20-2, pp. 19-21). It enjoys all the benefits of the ratiometric technique, plus improved linearity and superior sensitivity.

Connected to an ac-energized LVDT, it converts directly to 16-bit digital form without needing an intermediate analog voltage output. Its high input gain (up to 50×) and insensitivity to noise permit resolution in the nanometer (10^{-9} m) range with short-stroke LVDTs. For example, with a ±1-mm-stroke LVDT over a reduced range, the 2S58 can realize a resolution of 1.22 nm/LSB. Thus, it is useful for systems requiring precision linear measurement, including flight controls, machine tools (surface finish, contouring), even semiconductor wafer profiling. In addition, its nm-resolution capability makes the LVDT approach competitive with optical interferometric techniques.



HOW IT WORKS

The block diagram of Figure 1 illustrates one way an LVDT-to-digital converter can be applied. The LVDT consists of a transformer wound around an electrically isolated movable piston. The secondary consists of two opposed windings in series; and a constant-amplitude oscillator excites the LVDT's primary. When the core is centered, the secondary outputs are equal and their difference is zero. As it moves in either direction, there is a net ac output of appropriate polarity, with amplitude proportional to the deflection—over a range depending on the construction of the device.

The 2S58 compares the ac output with a reference derived by summing the secondary voltages (V_{REF}), using equal resistors, R1 and R2—and converts to digital, employing the tracking scheme of Figure 2. The ratio bridge determines the ratio of the difference to the (constant) sum and compares it to the digital value at the counter output; the ratio output is an ac error voltage, which is demodulated in the phase-sensitive detector, integrated, and converted to frequency in the voltage-controlled oscillator (V/F converter); each count causes the counter to increment or decrement—in the appropriate direction to reduce the error. Since the only steady state is when there are no pulses to count (zero VCO input [integrator output]) and no change in the integrator output (zero integrator *input* [error]), the loop tracks continuously, always seeking to maintain zero error between the digital word and the ratio of V_1 to V_{REF}; the loop can track signals with bandwidths up to 300 Hz.

The ratiometric design means that the 2S58 is insensitive to changes in the excitation voltage, frequency, and waveshape. Thus, high-stability oscillators need not be used. The tracking loop also has high noise rejection, so the device's user-programmable gain range (×10 to ×50) is fully available for real-world applications. The digital output continuously follows the transducer input without the need for external *convert* commands; a BUSY pulse is emitted while the data is changing to indicate its unavailability for transfer via the 3-state outputs.

The 2S58 is housed in a hermetic metal DIP, 2.14" × 1.14" × 0.18" (54.4 × 29 × 4.6 mm). It is available for both 0 to 70°C and −55 to +125°C operation. Prices start at $980 (25-99).

The 2S58 was designed by Matthew Finnie at ADI's Memory Devices division in East Molesey, UK.

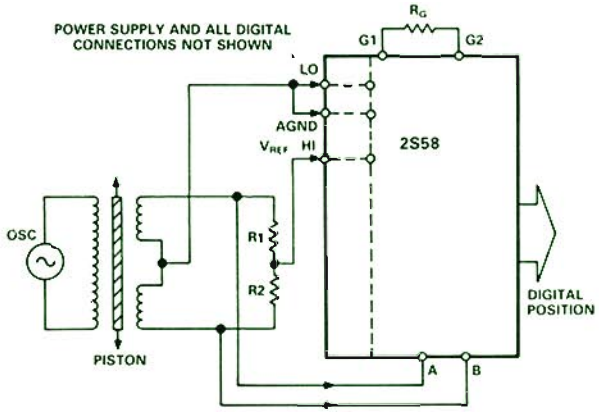


Figure 1. Three or four-wire LVDT connection.

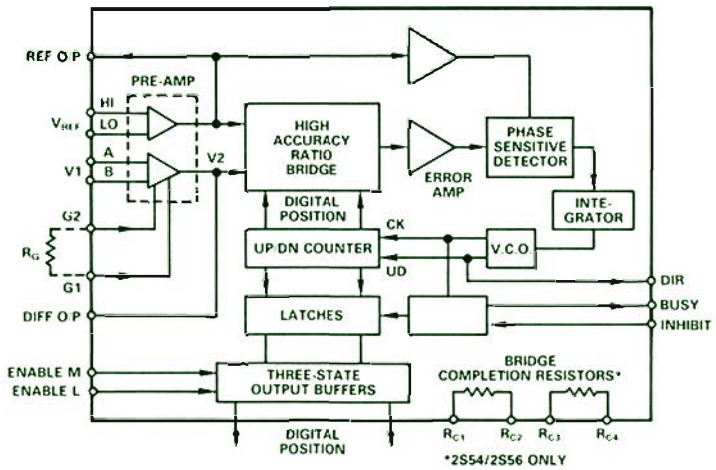


Figure 2. Functional block diagram of LVDT-to-digital converter.

*Use the reply card for technical data.

PORTABLE μP-CONTROLLED SYNCHRO SIMULATOR & TESTER

6S04 Digital Director Simulates Synchro Coarse-Fine Transmitters And Control Transformers; Displays Synchro Angular Position

The portable microprocessor-based 6S04* Universal Synchro Simulator and Test Instrument simulates synchro transmitter electrical outputs and tests synchro-input equipment. It is useful wherever synchros are employed, for example: servo-control systems, ATE systems, measurement of backlash in servo system gearboxes, and test of digitally controlled machines. Also known as a Digital Director, it is a modern version of a predecessor electronic "dummy director unit" (DDU)† developed some years ago for off-line testing of the synchros used in naval gun-control equipment.

It comprises three essentially autonomous units (Figure 1):

- A "*director*" simulates the electrical outputs of a 2-speed synchro coarse-fine transmitter.† The user can program the output of the director for either a fixed angle, manual control, or a choice of sine-wave, square-wave, constant-velocity, or square-wave-plus-velocity waveforms. The director has a synchro voltage resolution of 0.01% of output and angular accuracy to within ±0.15° at 15 VA output (400-Hz reference), and 0.1° at 5 VA output (60 Hz).
- An *angle position indicator* (API) measures and provides a front-panel display of angle as computed from signals in synchro format provided either by the director or an external synchro transmitter.
- A *solid-state control transformer* (SSCT) simulates the action of a conventional synchro control transformer by generating an analog signal proportional to the angular difference between the director output and the input from an external synchro transmitter.

The *director* consists of two electronically geared transmitters, each capable of driving a synchro transmitter with an accuracy to within 0.1° under full-load conditions. They are used in testing

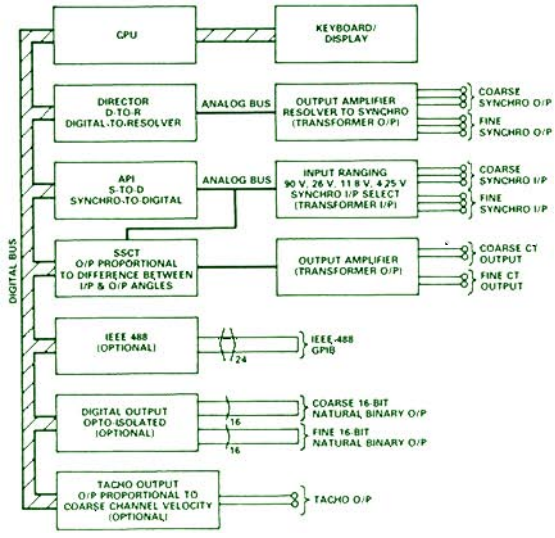


Figure 1. 6S04 functional block diagram.

*Use the reply card for technical data.

†Considerable information, historical and practical, about synchros & resolvers (including two-speed)—and peripheral subsystems, such as DDUs—can be found in the book, *Synchro and Resolver Conversion*, published by Analog Devices (1980) and available for $11.50.

two-speed synchro system, where one synchro is measuring a "coarse" position, and the other, geared to it, and rotating at a precisely related lower speed, is measuring a "fine" position; the two measurements are combined to obtain a considerably higher resolution than either one can provide by itself. The combined accuracy of the two signals is determined by the gearing employed. The voltages are either at standard 90-volt rms synchro levels for both coarse and fine, or in SLAB format—4.25 V rms on coarse and 11.8 V rms on fine.

The output functions of the *director* include:

- any angle, 0.00° to 359.99°; 0.1° accuracy and 0.01° resolution
- rotation either way at constant rates, from ±0.01°/s to ±359.99°/s
- sine or square wave, 0 to 100-s period, 0.00° to ±179.99° amplitude; square wave: starting angle from 0.00° to ±359.99°, sine wave: centered at any angle from 0.00° to ±359.99°
- constant rate plus square wave
- manual control, from 0° to 90°/s, on a log scale; can step forward or backward in preselected amounts, 0.00° to 179.99°; stepping can also be superimposed on constant rate.

The *angle position indicator* may be set to measure either the *director*'s angle output or the angle input to the instrument from an external synchro transmitter. Four selectable input ranges include: 90, 26, 11.8, and 4.25 V rms. Coarse, fine, or combined angle may be displayed, updated three times per second.

The *solid-state control transformer (SSCT)* provides signals from both the coarse and fine channels, to indicate the angular difference between the *director* output and the input from an external synchro transmitter. The error signal is scaled to give 1 volt per degree of error. The null voltage is 150 mV max, corresponding to 0.15° accuracy.

Available options include (1) an IEEE-488 standard 24-wire General-Purpose Interface Bus, which permits any standard IEEE controller to operate the unit (talk or listen) remotely; (2) a digital output consisting of two parallel 16-bit data channels, automatically updated with the coarse and fine output angles; (3) a tachometer output, in the form of an analog output signal via a BNC connector; it measures coarse angular velocity.

The 6S04 design team consisted of N. Webster, B. Duggan, and M. Caffrey, at ADI's Memory Devices division in East Molesey, UK.

CPU, SOFTWARE, & I/O INTEGRATED IN DISTRIBUTED CONTROL

μDCS-6000 Embeds Key Process-Control Blocks as Firmware With PC & FIX DMACS™ Software, It Provides a Seamless Solution

The μDCS-6000* combines the μMAC-6000* measurement-and-control system (*Analog Dialogue* 20-2) and FIX DMACS™ process-control software. This compounding of a hardware platform and applications software provides the user with a fully integrated, virtually "seamless" solution for personal-computer-based distributed control in factory automation.

No need for the user to write programs, just use menus to configure desired I/O software modules and database information; they are automatically linked together prior to actual execution on the hardware. A completed system includes a PC-compatible workstation (PC AT or PS/2-class), wired to up to 8 μDCS-6000 controllers via dual twisted-pairs as part of an RS-422 serial link; each controller can support up to 88 analog and 256 digital I/O points without adding μMAC-6000 slave units.

Each controller contains ROM-resident scan-, alarm-, and control software, enabling it to perform all I/O functions and communicate with the workstation in real time. A FIX DMACS software package residing on the PC provides supervisory control, user interface, process graphics, recipe-handling, and report logging, in collaboration with the μMAC-6000's advanced control functions, sequencing, and I/O.

The most-basic useful optional configuration of the μDCS controller and associated FIX DMACS software is for *supervisory control and data acquisition* (SCADA). Also available are upward-compatible ROM firmware and software for *control* and *statistical process control* (SPC). The basic *SCADA* functions include analog and digital I/O, frequency and event inputs, time-proportional outputs, and output ramping. The *Control* configuration adds PID

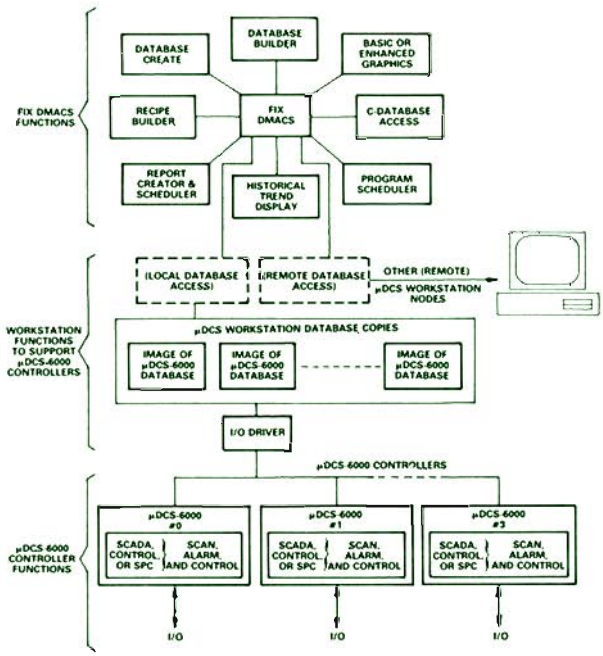
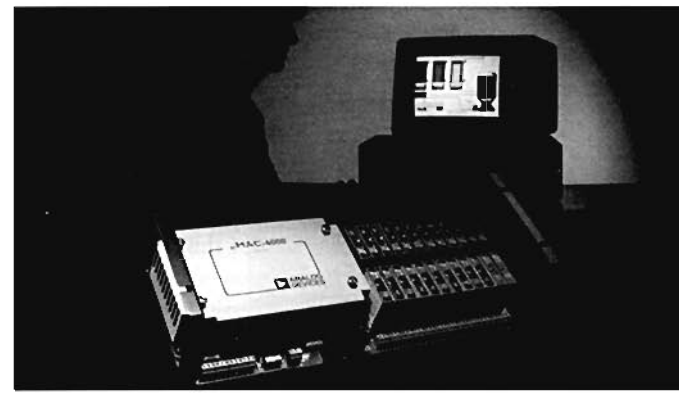


Figure 1. Functional Block Diagram of μDCS-6000 system.

*Use the reply card for technical data. FIX DMACS is a trade mark of Intellution, Inc. PC AT, PS/2, and NETBIOS are trademarks of International Business Machines Corp.



control—with enhancements, along with a program block for pre-defined macro functions for combined operations. Finally, the *SPC* version adds histograms and data analysis to the *Control* function.

Run-Time Mode: In operation, the system comprising the supervisory PC and μDCS-6000 provides all of the functions needed for powerful real-time process control; it combines widely distributed, autonomous local control with powerful user graphics and reporting—including charts, graphs, and tables. Special process-graphics makes it possible for these displays to use industry-standard symbols. Control parameters can be set, changed, and viewed from the keyboard, and controller-resident process parameters can be changed "on the fly" without cessation of the continuous operation of software control and monitoring. Multiple levels of password security are available.

The run-time mode also includes higher levels of supervisory control and interfacing; and it is compatible with IBM NETBIOS™ networking architectures. Multiple batch recipes can be set up in advance and downloaded automatically, as appropriate, from the supervisor workstation to the local controllers. Measured data from monitored points, both current and historical, can be called up and displayed in various formats.

Applications Configuration: The user builds the initial process database by selecting blocks from a menu; each block represents a required function, such as acquiring data, performing a calculation, or taking an action. The blocks are linked by using "tag names" of preceding blocks as inputs to subsequent blocks. Finally, the database is downloaded to the multidropped μDCS-6000 controllers. An application that is ready to run can be tested in simulation mode, verifying correct use of FIX DMACS, before downloading to the controller and going on-line.

System costs depend on the μDCS-6000 hardware configuration, the I/O modules chosen, and the software versions used. Typical software costs range from $5,600 to $11,600. A μDCS-6000 for SCADA costs $3,595 for the μMAC-6000 and special PROM (I/O modules separately). For the Control version, add $500, and the SPC version (including SCADA and Control) is $4,995.

Craig Brooke, at Analog Devices' Interface Products Division (Norwood, Massachusetts), was responsible for μDCS-6000 software, which integrates with FIX DMACS control software.

Worth Reading

BOOK REVIEW

Digital Signal Processing in VLSI, by Richard J. Higgins. *Published by Prentice-Hall in Fall, 1989. 614 pages. Available from Analog Devices @ $38 (use the book-selection reply card).*
Reviewed by Henry Davis.

"Do it digitally" is the opening exhortation in the Higgins text on digital signal processing (DSP). This book joins a growing number of works addressing the general subject of digital signal processing, but its approach sets it apart from others. Many existing textbooks are written for EE graduate or senior level students as part of their general EE curriculum. Such texts typically begin by jumping directly into the theoretical side of this applied mathematics subject. Higgins applies a combination of theory and practice to present a diversity of signal processing topics, without digressing into the proof of each key idea. Practicing engineers will find the general lack of mathematical proofs in Higgins's book a real plus; rules and key topics are introduced by application examples and summarized for convenience.

Chapter 1 sets the tone of the entire book. Although programming examples are included as a means to assist the computer scientist or software engineer in implementing DSP algorithms, the primary audience is defined by the use of analog real-world signal processing examples.

Electrical engineers should be very much at home with the introductory "Real-World Signal Processing." The chapter begins with an example that everyone should find familiar: the analysis of a room's acoustics in the time and frequency domains. Higgins goes on to suggest some potential applications of DSP in almost every application segment. Having established a conceptual framework, the text addresses fundamental issues of signal processing: signal-to-noise ratio, system models and transfer functions, time and frequency domain, and finally, the limitations of analog systems.

Each topic includes a real example; police radar is used as an example of both time domain (distance to target) and frequency domain (target speed via Doppler shift). Chapter 1 ends with an example of digital audio that touches on SNR, digital oscillators, digital mixers, equalization, reverb, independent tempo and pitch shifting, modems, speech synthesis, digital telephony, and digital audio restoration.

Chapter 2 sets out on a whirlwind tour of DSP basics for readers without the background. Higgins covers: signals and their frequency spectrum, convolution in Fourier transforms; sampled data theorem; DFT; poles, zeroes, and stability; the z transform. Altogether, either a good summary of DSP fundamentals for the beginner or a reference for the skilled engineer.

Chapters 3 and 4 complete the DSP background by covering digital Fourier transforms (DFTs), the fast Fourier-transform (FFT) algorithm, and digital filters. While not exhaustive in filter type or implementation strategy, these sections provide solid information regardless of your background.

Chapter 5 moves the discussion from principally generic statements to dealing with phenomena of real DSP implementations, including effects of finite wordlength, filter quantization errors, and accuracy in FFT spectral analysis. Higgins takes up the issue of DSP architecture and defines desirable features of a DSP processor. Finally, the chapter ends with the generally ignored subject of Analog I/O, including requirements and tradeoffs.

Chapter 6 completes the intellectual journey started in the first chapter by presenting examples of TI's '320' DSP microcontroller family and ADI's '2100' DSP microprocessor. Although manufacturers will continue to introduce DSP products, making this section somewhat sensitive to shifts in strategy, the concentration on the two most popular families of DSP makes this a valuable reference chapter for new product evaluations. Perhaps more importantly, it shows engineers how the concepts of DSP architectural requirements are applied with real-world products.

The realities of hardware implementation and development systems are covered in Chapter 7. By addressing the tools necessary for DSP development, Higgins rounds out a complete coverage of DSP for working engineers. The text is necessarily brief—but does a good job of describing the environment for those who have not completed a DSP or microprocessor-based design.

Providing applications motivation for DSP neophytes is always a challenge. The last chapter provides a collection of application examples drawn mostly from potential (and now real) products for consideration and discussion. Higgins's examples explore signal detection, image processing using CAT, PET, and MRI image reconstruction; real-time signal generation of musical instruments; and modeling in real-time for telecommunications and speech.

Digital Signal Processing in VLSI could have been entitled, "DSP Handbook for Engineers and Scientists." As a sourcebook for DSP professionals implementing real-world systems, Higgins rates a place on your technical bookshelf. If you're just embarking on learning DSP techniques, the book is among the best practical learning opportunities available. The addition of a problem-oriented workbook would make this an above-average college-level text for one or more courses in DSP.

Its sole potential weakness is the lack of detailed proofs of techniques. This lack is more than offset by frequent references to sources, an annotated Bibliography, and the richness afforded by the substitution of real-world *vigor* for mathematical *rigor*.

Henry Davis is a Product Line Manager in the DSP Division of Analog Devices, Inc., Norwood, Massachusetts

NOTED BRIEFLY (FREE, use reply card)

Application Note: "Considerations for Selecting a DSP Processor (ADSP-2100A vs. TMS320C25)" by Bob Fine.

Application Note: "Loading an ADSP-2101 Program via the Serial Port," by Gerald McGuire.

ADSP2100 Family Applications Handbook—Volume 3: Optimized and 2D FFTs; Memory Interface; Multiprocessing; Host Interface; Sonar Beamforming.

DSPatch—The Digital Signal-Processing Applications Newsletter, Number 12, Summer, 1989. Featuring "The Killer B's" (the 1.0-μm ADSP-1010B, the lowest-power 45-ns multiplier-accumulator available), also deglitching DACs, and much more.

Analog Briefings—The Newsletter for Military-Avionics Industry, Vol. 5, No. 2, 1989. Featuring MIL-Qualified Op-Amp Selection; High-Accuracy VFC (AD652/883B); and more—plus 6-page listing of all QPL, SMD, and MIL-STD-883 products from Analog Devices.

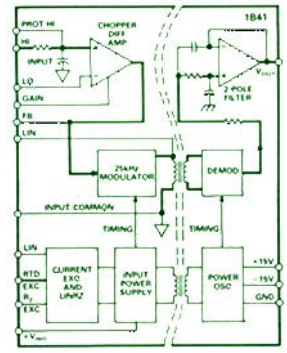
ISOLATED SIGNAL CONDITIONER FOR RTDs

1B41 Includes Excitation, Chopper Amplifier, Filtering, Lead-Resistance Compensation and 1,500-V RMS Isolation

The 1B41* is a complete signal-conditioning solution for RTDs (resistance temperature detectors); it includes current excitation, a low-pass-filtered and fault-protectable input, resistor-programmable gain, linearization, a chopper-stabilized amplifier, two-port isolation (1,500-V rms continuous), and a two-pole active output filter. It is housed in a small (1" × 2.1" × 0.35") DIP package.

Designed for use in data acquisition and industrial measurement-and-control systems, it is especially suited to harsh environments with extremely high common-mode interference. Unlike expensive solutions that require expensive dc-to-dc converters, each 1B41 generates its own floating current excitation, for low-cost channel-to-channel isolation.

Salient specifications include linearization with ±0.1% FSR conformance (100-Ω Pt),



low input offset tempco, 0.002 Ω/°C, and high common-mode rejection, 160 dB min at 60 Hz (1-kΩ source imbalance). The combination of input and output filtering provides 60 dB of normal-mode rejection at 60 Hz. The 1B41AN operates from −40°C to +85°C—and with rated performance from −25°C to +85°C. Its price is $58 (100s).

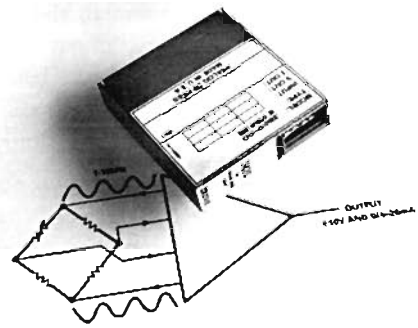
AC STRAIN GAGE 3B-SERIES INPUT MODULE

3B20 Interfaces to Strain Gages and Torque Transducers Configurable Gain—and Excitation Voltage & Frequency

The 3B20* is a complete signal conditioner for ac bridges. It provides excitation at frequencies from 1 to 10 kHz and voltages from 2 to 10 V rms at up to 20 mA rms. Accepting input signals with ranges from 1.5 to 150 mV rms, it provides high-level voltage and current outputs: ±10 V and 4-to-20 mA or 0-to-20 mA.

The proven and popular 3B Series Signal-Conditioning I/O Subsystem* (*Analog Dialogue* 16-3, 1982) provides a low-cost, versatile, modular method of interconnecting real-world analog signals to a data-acquisition, monitoring, or control system at standard input levels. This newest member of the series is a significant addition to the dozens of interfaces already available (with both standard and custom ranges), including various dc and ac voltage and current ranges, thermocouples, RTDs, strain gages, LVDTs, etc.

Specifications of the 3B20 include accuracy



to within ±0.1% of span; nonlinearity less than 0.05% of span; ±0.005%/°C zero stability for voltage output and ±0.0025%/°C for current output; span stability of ±0.01%/°C (voltage) and 0.0025% of reading/°C (current). The input and current outputs are protected against differential faults (continuous) of up to 130 V rms; the voltage output is protected against continuous shorts to ground. Prices start at $225 for single units; substantial discounts are available in large quantities.

*Use the reply card for technical data.

ISOLATION AMP

For −55°C to +125°C Single-Supply AD203SN

The AD203SN* is a two-port, MIL-temperature-range transformer-coupled isolation amplifier designed and built for use in hostile operating environments; it is packaged in a 2.23" × 0.83" × 0.58" DIP and operates from a single 15-volt (±5%) supply. Its price is $58 (100s).

It galvanically isolates the input from the output, eliminates ground loops, rejects high common-mode voltages and common-mode noise, and protects sensitive electronic signal-processing systems from upstream transient and/or fault voltages.

Typical applications include engine monitoring and control, mobile multichannel data-acquisition, isolating instruments and control systems from signal sources, current-shunt measurements, and measuring small voltages at high levels. It should be especially useful in military and heavy-duty industrial and transportation electronic equipment.

The AD203SN provides 1.5 kV rms of common-mode isolation, 10-kHz full-signal bandwidth, and a buffered ±10-volt output range. It handles full-scale input ranges from ±100 mV to ±10 V and provides up to 150 mW of isolated front-end power. Its uncommitted input amplifier can be connected for gains from 1 to 100 V/V, or in other op-amp configurations.

This latest descendant of the proven AD202 series of isolators (*Analog Dialogue* 20-1, 1986), is characterized to work within specifications over the entire −55 to +125°C operating temperature range; in addition, it is designed and packaged to meet a series of stringent environmental tests outlined in MIL-STD-883C for moisture resistance, temperature cycling, mechanical shock, lead integrity, variable-frequency vibration, and resistance to solvents.

Ask The Applications Engineer—4

DISK-BASED COMPONENT SELECTION GUIDE SEEKS BEST CHOICES

User's PC (or Compatible) Searches the Data Base Between Min/Max Specs

Tradeoff Among Parameters is Visible; Choices are Ranked by Ascending Price

by Bill Schweber

Question: You have the largest selection of great products in the industry. But I go nuts trying to find the lowest-cost solution with the best set of specs for my job. HELP!!

Your job just got easier. Analog Devices now has a FREE easy-to-use solution to the first step of identifying which components from its extensive catalog are suitable for a design—and tradeoffs that can be made. The *Components Selection Guide** is a multiple-parameter searchable data base following the format of the 74-page *Short Form Designers' Guide** The 5.25" disk runs on virtually any PC or -compatible running DOS and needs no special training. Its label instructs, simply: "Boot to DOS for prompt. Type ADI (return) or ANALOG (return) to run."

The disk-based selection guide prompts the user to enter the desired minimum and maximum specifications for key parameters in a component category. A single keystroke initates a search through its database to find all model numbers that fall within the defined boundaries. The lowest-priced of these models are displayed, along with their key specifications, in order of ascending user cost. The design engineer can get a printout of the screen and use it to find data sheets of the most likely candidates in the component databooks to continue the design process.

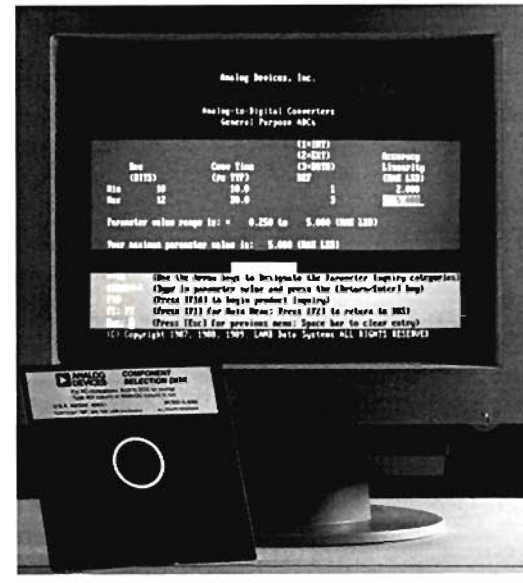
A significant part of the engineer's responsibility is to select the "best" component for the design application. But it's often a frustrating task, since major vendors offer a wide spectrum of components, with superior performance in some key specs (such as speed, resolution, accuracy) and lesser performance in others.

Without this tool, the proliferation of products often leads the designer to make a suboptimum choice. The traditional method of searching through a component catalog tends to undermine the engineer's confidence that, in the time available, the final selection was the best—and inhibits the process of making intelligent tradeoffs in component cost-versus-performance in the context of the overall system design. Where such tradeoffs are visible, an engineer may use a component with lesser specifications to reduce cost, and compensate for its inadequacies elsewhere in the design; conversely, (s)he may decide that a small cost increment buys enough improved performance to justify the difference while simplifying the rest of the design. In the absence of this tool, some designers, pressed for time, may simply use a familiar product (good enough but not the best choice).

EXAMPLE OF A SEARCH

To start, simply type in 'ADI' (return) or 'ANALOG' (return), depending on the computer's screen graphics—VGA, EGA, or "Hercules". Suppose the designer needs a general purpose a/d converter (ADC). After the initial logo and "user notice" screens, the major component categories appear (Figure 1). They are identical to those in the printed *Short Form Designers' Guide.*

The ↑ and ↓ are used to select the desired category. For ADCs,



following the printed *Guide*, there are subcategories, which come up on a new screen (Figure 2). Again using the arrows, we select the category 'General Purpose ADCs.'

The next screen (Figure 3) shows the ease of use and power of the searchable data base. Four parameters appear for which the user can enter minimum and maximum values: resolution (bits), conversion time, reference type, and accuracy/linearity (which blends both specs into an overall summary performance level). As each parameter field is highlighted, the screen shows the available minimum and maximum value of the parameter in the subcategory; an out-of-range message is shown if the user-entered value exceeds the bounds. With this feature, the user does not waste search effort asking for a 6-bit device when there are no ADCs with this resolution available in the category.

The fields do not have to filled in a specific order. (Indeed, a default search can be made without a single entry.) With the arrow keys, the user goes from field to field in any sequence. The example shown requests resolution between 10 and 12 bits, conversions times from 10 to 30 μs, internal or external reference, and accuracy/linearity from 0.5 to 2 bits. If there is a parameter whose maximum or minimum specifications are not relevant in the application, just leave the field blank. The search algorithm automatically fills in the category's max or min value.

With the parameters chosen, the user hits the PC's F10 function key. Within seconds, the results are displayed (Figure 4): the actual model numbers—not just the generic product numbers—and their key specifications. The first component listed is the least expensive; each following one is as costly as or more costly than its predecessor. Note: the results include 10- and 12 bit, 10 to 25 μs, 0.5 to 2-LSB-error devices; all fit within search bounds.

If no component entry in the data base is found simultaneously to meet the multiple dimensions of the parameter search, the search

*Use the reply card to obtain a copy.

algorithm automatically begins to expand the specifications limits by small percentages. When it does find components that meet all the expanded criteria, it stops the search and displays the results. Since the designer sees which parameters were stretched and the resulting specifications for the chosen parts, he or she can determine if this combination is appropriate for the application.

Why minimum *and maximum?* By establishing both min *and* max specifications for each parameter, the database avoids some obviously inappropriate choices. For example, if an 8 to 10 bit ADC is needed, but the only bound to be established is the *max* conversion time, a designer looking for a relatively slow and inexpensive ADC might also find costly, irrelevant 8-bit, 300-MSPS devices. Instead, both upper *and* lower bounds are imposed for each performance dimension.

A screen can be printed by using the PRINT SCREEN key, supported under DOS, for a permanent record of the listing of selected devices as a design milestone. Normally, the design engineer will use the results as a guide to design, starting with the least expensive device that meets the requirements. *The disk-based selection guide is not intended to replace individual component data sheets*; the engineer must use them to compare component performance and design requirements for parameters and characteristics not included in the disk data base.

The ease with which specifications are entered allows the engineer to ask some "what if?" questions. For example, suppose, based on initial analysis, 2-LSB is the maximum acceptable error value. If the result of the search inquiry turns up only components that are too slow, for example, the user can go right back to the parameter entry screen to try again simply by hitting the ESCAPE key (from Figure 4 back to Figure 3).

Reentering *only the specification to be changed*, the user now increases the limit for maximum accuracy/linearity error from 2 to 4 LSB, and quickly sees what is available—all other spec entries are unchanged. Perhaps a faster device can be utilized, with its additional error ultimately calibrated out via system software.

In the subcategories, the most appropriate parameters and units are used for defining the component performance. For example, general-purpose ADCs usually specify conversion time in μs, while flash converters use sampling rate in MSPS. Accordingly, the ADC subcategory of "video ADCs" uses MSPS, while the general-purpose ADC subcategory uses μs. Designers looking for general purpose ADCs don't have to translate their μs needs into awkward equivalents of megasamples per second (with a relatively slow 20-μs conversion time reading: 0.05 MSPS!).

Certain parameters are unique to specific subcategories of a given category; e.g., "sample-and-hold bandwidth" is meaningful only for *sampling* ADCs; so it is listed just for that category.

The *Component Selection Guide* will also display key specs in response to a model number. Simply key it in, e.g., AD844AN; the disk searches its entire data base to find and display the part's specifications, regardless of the category in play; for example, op amp specs can be found while ADC choices are up.

The Analog Devices *Component Selection Guide* is not copy-protected; duplication onto another floppy or a hard disk is not restricted (perhaps even welcomed as spreading the 'word'). The data base and search program* are 'sealed' against user-initiated changes to avoid susceptibility to error, bugs, or viruses). ◘

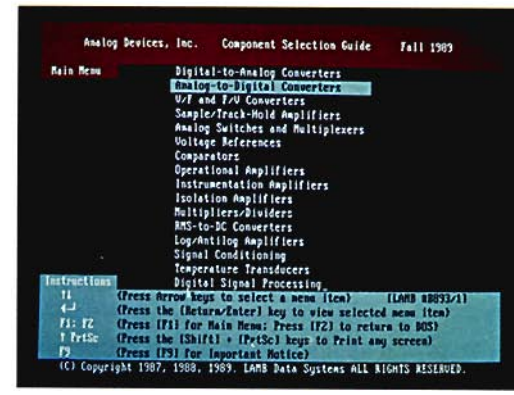


Figure 1. Initial search screen shows all major product categories.

Figure 2. Subsequent screen shows subcategories for a/d converters.

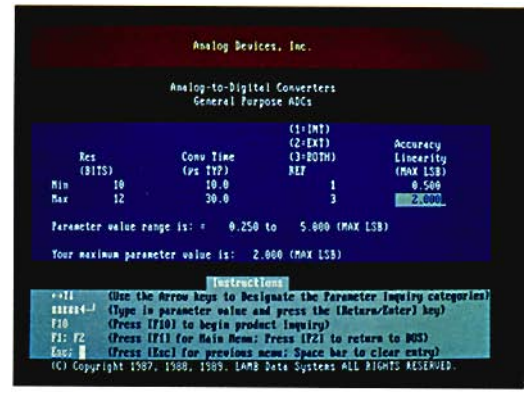


Figure 3. Screen for user entry of minimum and maximum performance parameters for general purpose a/d converters.

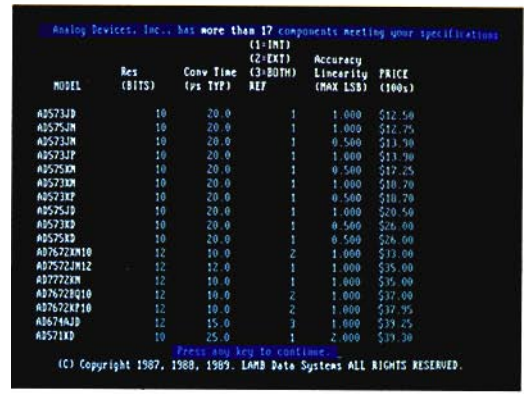


Figure 4. Screen showing suitable components with their specifications—in order of ascending user cost (based on U.S. prices).

Across The Editor's Desk

CURRENT FEEDBACK AND TRANSIMPEDANCE

A reader writes:

"I read with interest the article on page 13 of Analog Dialogue 22-2. I have recently been working with transimpedance amplifiers and do not understand them. I have been using the conventional op amps in the current feedback mode and have assumed that this is the same as a transimpedance amplifier. After reading your description of the AD846, I wondered what characteristics an amplifier must have to be called as a transimpedance amplifier. Can you enlighten me as to what a good transimpedance amplifier should do and whether capacitance on the null junction has any effect on the bandwidth?"

A *current-feedback amplifier configuration* is one in which the feedback signal is developed as a current, which is added to or subtracted from a current in the input stage. A simple example of a current-feedback amplifier is a single FET connected as a *source follower* with a resistive load; it feeds back a current equal to the output voltage divided by the load resistance. A source follower is characterized by high input impedance, very nearly unity gain, and low impedance at the feedback point; its output voltage is essentially independent of load variations. Many kinds of current-feedback circuits are possible.

A *transimpedance operational amplifier* is a special kind of op amp that responds to a current at its normal inverting input and produces a voltage at the output. That's different from the more familiar op amp, which responds to *voltage* and has a voltage output. Here is how their properties compare:

"Gain" relationship	$V_{out} = -A\ V_{in}$	$V_{out} = -Z_t\ I_{in}$
"Gain" characteristic	V/V (voltage gain)	V/I (transimpedance)
Ideal value of "gain"	$A \rightarrow \infty$	$Z_t \rightarrow \infty$
Ideal input impedance	$Z_{in} \rightarrow \infty$	$Z_{in} \rightarrow 0$
Input error current, I_{in}, for normal V_{out} when used in ideal feedback amplifier	$(V_{in}/Z_{in}) \rightarrow 0$ (high impedance)	$(-V_{out}/Z_t) \rightarrow 0$ (high "gain")
Input error voltage, V_{in}, for normal V_{out} when used in ideal feedback amplifier	$(-V_{out}/A) \rightarrow 0$ (high gain)	$(I_{in} \times Z_{in}) \rightarrow 0$ (low impedance)

Both types of amplifier will make a good op amp, because both maintain zero input voltage and current. The principal difference is as follows: the voltage-to-voltage op amp works by using voltage feedback to maintain a voltage null (while its net input current, being zero because of near-infinite input impedance, forces all currents to flow only among the operational impedances); the transimpedance op amp works by using current feedback to maintain a current null (while its input voltage, being zero because of near-zero input impedance, forces the summing node to be at "ground" potential).

From this it can be inferred that transimpedance amplifiers have the potential advantage that they tend to be less sensitive to capacitance at the summing point because of the inherently low impedance level.

While the above discussion is qualitative and somewhat intuitive, we hope our reader(s) will find it helpful as a first step towards understanding (a) the difference between transimpedance op amps and normal voltage-gain op amps, and (b) that the transimpedance op amp is an amplifier optimized for current-feedback circuits.

P.S. Does this discussion help you understand that a conventionally designed high-input-impedance op amp (especially a FET-input type) *can't* be used in the current feedback mode (connecting only to its usual terminals, and with non-floating supplies) because it responds to *voltage* and sees current only as a leakage? Nevertheless, it can be programmed through its external *operational circuitry* to perform all sorts of current transformations, V-to-I, I-to-V, and current amplification—but these properties derive from *voltage-feedback* operations. ▶

MORE AUTHORS *(continued from page 2)*

David Duff (page 10) is Product Manager in Strategic Marketing at ADI's Computer Labs Division. He received a BSE from the University of Tennessee, MSEE from Georgia Tech, and MBA from the University of North Carolina. He joined Analog Devices in 1982. In his spare time he enjoys downhill skiing and sailing.

Bill Sheppard (page 11) is a Marketing Engineer in the Interface Products Division (IPD) of Analog Devices. Since joining ADI in 1969, he has held positions as Test Supervisor and Quality-Control Supervisor. In his present position, he supports IPD's High-Resolution Converter product line and pin signal conditioners. He received his ASET at Brevard Junior College in Cocoa, Florida. His hobbies include golf, fishing, and high-performance Buicks.

Pete Predella (page 13) is a Technical Publicity Associate at Analog Devices, in Norwood MA. Since joining ADI, in 1979, he has also been a Technician for the Component Test Systems and Memory Devices Divisions. Peter is a graduate of GTE Sylvania Technical School and is currently pursuing a BSET from Northeastern University. His interests include reading, salt-water fishing, and golf.

Bill Schweber (page 7) is a Senior Technical Marketing Engineer and Contributing Editor to *Analog Dialogue*; he spearheaded the *Disk Selection Guide* and was also responsible for several other articles in this issue. Besides having his BSEE and MSEE degrees, he has designed μP-based machine controls, been a product marketing engineer, authored numerous technical articles, and written two textbooks. He enjoys bicycling and reading. ▶

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

IN THE LAST ISSUE

Volume 23, Number 2, 1989, 24 Pages

Editor's Notes, Authors
Advanced Microcomputer Is Optimized for DSP (ADSP-2101)
Converter/Filter Chip Set for Voiceband Applications
Isolated Strain-Gage Module Joins 5B Series Conditioner Family
6-Bit Monolithic Flash ADCs Sample at up to 500 MHz (AD9006/16)
Fastest-Slewing Monolithic Op Amp Has Wide Bandwidth (AD844)
Fast, Low-Power Op Amps Offer Gani-Bandwidth Choice (AD848/9)
Enhancements to LTS-2020 Benchtop IC Tester
New-Product Briefs:
16-Bit ADC Converts in 10 µs (AD1377)
TTL-Compatible Programmable Digital Delay Generator (AD9501)
16-Bit Sampling A/D Converter, 50-kHz Throughput (AD1380)
C Compilers for ADSP-2100 Programs
Monolithic Quad 12-Bit DAC is MIL-STD-883-Qualified (AD664)
45-ns 16 × 16-Bit Multiplier/Accumulator (ADSP-1010B)
Ask the Applications Engineer—3: V/F Converters
Worth Reading
New Fellow Named at Analog Devices: Fred Mapplebeck
Potpourri
Advertisement

ERRATA: . . . ***Analog Dialogue*** 23-1, page 8, Fig. 2: +5 V and -5 V connections are interchanged . . . 23-1, page 10, Fig. 2a: AD9901 block diagram, oscillator input flip flop. Q connects to lower input of XOR, $\overline{Q}$ connects to D, no dot at crossover. Same error on page 1 of AD9901 data sheet (pub. C1272-10-2/89). . . . 23-1, page 10, Fig. 2b: AD9901 waveforms, dashed line through XOR gate output should be labeled DC mean value (not rms). Same error on pages 7 and 8 of data sheet, Figures 2, 3, and 4 . . . 23-2, page 6, Greg Koker formed and now heads the ADSP-2101 design team . . . In the **1988 *Data Conversion Products Databook***, pages 2-27 and 2-35, AD394, AD395, AD396, package option is DH-28A, 28-lead bottom-brazed hybrid package (not side-brazed DH-28); also, page 2-21, AD392: package option is DH-32A, 32-lead metal platform DIP, not DH-32E; also, page 2-295, AD9702: package option is D-24, not D-24A.

PRODUCT NOTES: . . . **New Data Sheets.** Composite data sheet for 2B Series Two-Wire (current) Transmitters includes: 2B24, loop-powered isolator and the following temperature transmitters—2B52/53 (for thermocouples), 2B57A-1 (for AD590), 2B58 (linearizing, for RTD), 2B59 (low-cost, for RTD). Ask for C1185-15-7/88 . . . New and improved AD9005 (12-bit, 10 MSPS ADC) specs include lower harmonic distortion and higher SNR at 540 kHz, 2.3 MHz, and 4.3 MHz, lower differential nonlinearity, and reduced power dissipation. Request C1219a-10-5/89 . . . **Other:** If you have an early evaluation board for AD9005, make sure pins 6 & 7 of U4 are connected together . . . AD7582's differential nonlinearity spec is now ±1 LSB max; no-missing-codes performance is guaranteed (20% guard band) . . . There are new specs on output delay and positive supply current for AD9012, and on positive supply current for AD9048. Consult your local sales office.

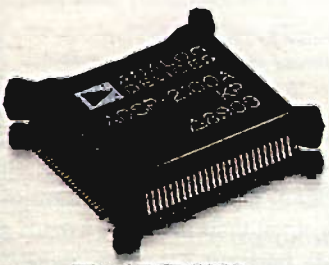
UPDATE . . . **ADSP-2100 news:** ADSP-2100 Demo disk for IBM PC available from your nearby sales office (unrestricted copying) . . .A training course is available to accelerate your development of ADSP-2100 projects, "System development and Programming with the ADSP-2100 Family." Ask your local sales engineer for schedules and costs . . . ADSP-2101 cross-software tools (rev 2.0X) are now available for the IBM PC; the package includes the system builder, assembler, linker, prom splitter, simulator, and C compiler. Simulator includes windowing features. Check with your local sales office (CWYLSO) . . . ADSP-2100A small-quantity prices have dropped. CWYLSO . . . **Elsewhere:** Surface-mount CMOS DACs, ADCs, switches/muxes, and other products are available in tape and reel packaging for large-volume users; it's an efficient way of providing material to pick-and-place machines. CWYLSO . . . Many devices are available in chip form for hybrid circuits. For information, CWYLSO . . . µMAC-6000 prices are coming down . . . So are AD9005's. CWYLSO.

MILITARY ROLL CALL . . . A 12.5-MHz version of the ADSP-2100, the ADSP-2100AU, is now available with MIL-STD-883B processing. Its 80-ns instruction cycle, dual-port Harvard architecture, and zero-overhead branching and looping (2.94 ms for a 1K complex FFT) make it arguably the fastest programmable DSP available for military applications. It will soon join the other versions of the ADSP-2100 on Standard Military Drawing (SMD) 5962-87735. It is optionally available in a 100-lead compact surface-mountable CQFP (ceramic quad flat pack). CWYLSO . . . The highest-performance monolithic V/F Converter is now available to MIL-STD-883. Ask about AD652SQ/883B . . . The AD573 and AD673 8- and 10-bit ADCs with µP interface are now available on Standard Military Drawing 5962-88505. Ask for respective part numbers 5962-8850501RA and 5962-8850502RA.

PATENTS RECEIVED . . . 4,833,345 to Gerald A. Miller for Sample/Hold Amplifier for Integrated Circuits . . . 4,839,653 to Lawrence M. DeVito for High-Speed Voltage-to-Frequency Converter.

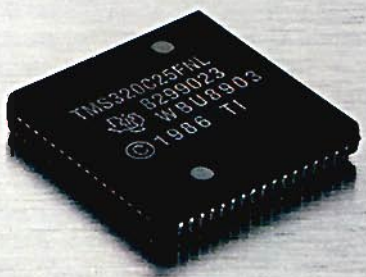
"CWYLSO" = Check with your local sales office.

Given enough time, the TMS320C25 can do almost everything the ADSP-2100 can.



The ADSP-2100.

- The ADSP-2100 computes a 1024-point complex FFT in less than 3 ms with a total memory requirement of less than 4k bytes. It also computes a 2 × 2 2D convolution in 1.2 μs and executes ADPCM in only 68 μs.
- The ADSP-2100 can access two words of external data every cycle.
- The ADSP-2100 supports zero-overhead loops of any length. So our looped code – which is the easiest to write – is also the fastest.
- The ADSP-2100's two dedicated data address generators can auto-increment/decrement by any offset value, and they have automatic circular buffer wraparound.
- The ADSP-2100 Assembler supports the easiest language in the business. So you code a multiplication/accumulation the same way you'd write the original algorithm. For example, the algebraic R = R + X*Y codes as MR = MR + MX0*MY0.



The TMS320C25.

- The TMS320C25 takes more than three times as long to compute the same size FFT, while it devours over 47k bytes of memory.[1]
- The TMS320C25 is limited to one access of external data every two cycles.
- The only zero-overhead loop the TMS320C25 can execute is one instruction repeated no more than 256 times.
- Circular buffers? The TMS320C25 doesn't support them.
- The TMS320C25 is programmed with 133 mnemonics like SPAC, BGEZ, MACD, XORX, and SBRK. A multiplication/accumulation is coded as MACD >FF03;*–. While this might not scare the XORX out of you, it's not the easiest thing to debug or maintain.

We're not saying the TMS320C25 is slow. But even if it were twice as efficient as it is now, it'd still be a lot slower at DSP than the ADSP-2100. The fact is, the ADSP-2100 is out in front of the TMS320C25 in performance, readability of code, and development tools.

Just how far out front? Get our free technical booklet and read about it. Or better yet, get an ADSP-2100 sample kit for only $49.95 and see for yourself. To request either, call DSP Marketing at 1-617-461-3771.

ANALOG DEVICES

Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; Headquarters: (617) 329-4700; California: (714) 641-9391, (619) 268-4621, (408) 559-2037; Colorado: (719) 590-9952; Maryland: (301) 992-1994; Ohio: (614) 764-8795; Pennsylvania: (215) 643-7790; Texas: (214) 231-5094; Washington: (206) 575-6344; Austria: (222) 885504-0; Belgium: (3) 237 1672; Denmark: (2) 845800; France (1) 4666-25-25; Holland: (1620) 81500; Israel: (052) 911415; Italy: (2) 6883831, (2) 6883832, (2) 6883833; Japan: (3) 263-6826; Sweden: (8) 282740; Switzerland: (22) 31 57 60; United Kingdom: (932) 232222; West Germany: (89) 570050.

[1]EDN, "EDN's DSP Benchmarks," September 29, 1988.